http://www.commsdesign.com/news/showArticle.jhtml;RVVRCYNNMZRVGQSNDLOSKHSCJUNN2JVN?articleID=193005379

Alpine lab enters rarified air of soft-error test

By Junko Yoshida
EE Times
Sep 25, 2006

GENEVA — Investments in time and dollars notwithstanding, semiconductor soft errors remain a tough nut to crack.

Certainly, scientists and engineers have known for decades that soft errors, which occur as a result of cosmic radiation, can alter the state of the circuit, causing systems to malfunction unpredictably. The industry has even jury-rigged a few remedies to shrink soft error rates (SERs), applying them in DRAMs, SRAMs and chips targeted at space-borne applications.

But the accuracy of current methods for SER modeling and test is a lingering unknown. Most manufacturers jealously guard test results, making it tough to draw useful comparisons and conclusions on SER data collected so far. And nobody knows how well current SER predictions will hold up under the next process node's finer geometries.

Some clues could be forthcoming this week, when an emerging test program announces its preliminary results in Athens at the Radiation Effects on Components and Systems (Radecs) technical conference. Since March, STMicroelectronics and the Laboratory for Materials and Microelectronics of Provence (L2MP) have been quietly conducting real-time SER testing of semiconductor memories at a site in the French Alps, at an elevation of 2,552 meters, under Europe's Altitude Single-Event-Effects Test European Platform (Astep) program. Intending eventually to open its facility to the industry, Astep has also brought in Xilinx FPGAs to test.

Through real-time soft-error testing at high altitudes, Astep hopes to add another data point to the established suite of approaches for estimating SER. Those current methods include accelerated alpha-particle and neutron or proton source/ beam testing; life testing in natural environments; and modeling and software simulation at the device or circuit level.

An important advantage of high-altitude facilities is that "upsets happen from five to 15 times more often, depending on altitude, thus generating better data, sooner, with less uncertainty," said Austin Lesea, principal engineer at Xilinx Inc.

"Use of high-altitude testing stations more closely mirrors a 'real world' application, compared with bombarding a sample with radioactivity to simulate the conditions a

part would see in the real world," said Richard Wawrzyniak, senior analyst at Semico Research Corp.

Additional real-time SER testing is "critical to giving our customers scientific confidence in the robustness of our chips," said Jean-Pierre Schoellkopf, director of advanced design, central CAD and design solutions at STMicroelectronics. Astep's mission, he said, is to prepare for what SERs may look like "10 to 15 years from now."

Leaving no trace

SERs are "a tricky phenomenon to study and model," said Olivier Lauzeral, general manager at iRoC Technologies Corp. Occurrences are rare, making SERs difficult to observe. Worse, "they don't leave any physical trace in the chip that could allow for postmortem investigations," Lauzeral said.

SER testing deals with many probable events, including the "locations of the collision of particles with silicon atoms, the energy involved, the by-products created and the charges deposited," Lauzeral said. The litany of potential unknown factors tends to render SER predictions and even artificially accelerated tests "prone to errors," he said. Maximizing prediction accuracy thus requires "a large amount of test data points, correlated with simulation and a comparison with real-time, nonaccelerated testing," Lauzeral said.

Bob Patti, chief technology officer of Tezzaron Semiconductor Corp. (Naperville, Ill.), lamented the lack of modeling tools to gauge SER interactions in materials. Further, he said, current testing doesn't test circuits at speed. Citing the generally slow, FPGA-driven speeds for SER testing, he said, "If the circuit is given enough time to recover, the error just disappears. We can't model, and the testing methodology is flawed."

Currently, the most widely applied approach to characterizing SER uses alpha-particle sources and neutron beams with high intensity. In a recent paper, Xilinx researchers wrote that "beam testing is not accurately predicting the real improvements that are being realized in atmospheric testing."

"Actual atmospheric data is absolutely essential," Xilinx's Lesea said, "as beam testing has now been shown to be pessimistic by factors as great as five to eight."

Tino Heijmen, senior scientist with NXP Semiconductors's Corporate Research unit, agreed that "extrapolating accelerated SER data to nominal use conditions can result in large overestimations." For Heijmen, accelerated testing becomes a big- ger headache as technology scales: "More and more library cells become sensitive to radiation. It's not feasible to characterize the SER of all of them with accelerated testing."

SER test of nonmemory elements, meanwhile, "is complex because the results depend on the test conditions," Heijmen said. For such cases, SER models can provide a useful alternative, provided they are calibrated with experimental data, he said.

Even if SER effects can be properly modeled, the challenge remains to design circuits that circumvent or tolerate SERs. As chip densities rise and low-voltage requirements mount, iRoC's Lauzeral said, "there is a need for low-area-, low-consumption-impact solutions that can be implemented early on in the design of devices, at the front-end level."

Lofty goal

Astep's lab, situated on the Pic de Bure in the French Alps, is small and still undergoing validation. The lab is equipped with homegrown universal SRAM automatic test equipment that can monitor several thousand synchronous and asynchronous SRAMs simultaneously as data is read from and written to the chips. The ATE also compares output data with written data and records details on the different detected errors.

The lab's ATE has been running at full capacity--testing 1,280 memory chips in four racks—since May.

Because the immediate mission of Astep is to validate its system against previously collected SER data, the program's first life testing has been performed on bulk SRAM devices fabricated by ST using a 130-nanometer commercial process. ST plans to initiate real-time SER measurements by year's end on 1,200 units of 8.5-Mbit SRAMs manufactured in 65-nm commercial CMOS.

The lab at Pic de Bure currently houses only ST SRAMs and Xilinx FPGAs. Astep, however, aspires to transform its lab into "an industrial structure that will be open to the public," possibly in 2007, according to ST's Schoellkopf.

ST reported that the lab's ATE detected 11 single-event errors in the first month of operation and a total of 15 errors in the two-month preliminary period. Statistical formulas convert that data to a soft-error rate of 600 failures in time (FIT)/Mbit. That means 600 failures can be expected in 1 billion hours of operation per 1 million bits of memory.

Although the data is still preliminary, ST's Schoellkopf said the result is "fully in line with our expectations for other combined accelerated and real-life SER experiments previously reported in the literature."

Having several such altitude stations could prove "valuable in the process of securing results," said Marc Derbey, president and CEO of iRoC Technologies (Grenoble, France).

Indeed, Xilinx is gathering results from seven sites, six of which are used to gather "real, atmospheric failure rates," said Lesea. Those six sites are San Jose, Calif.; Albuquerque, N.M.; California's White Mountain Research Center; Mauna Kea, Hawaii; Marseilles, France; and Pic de Bure. The seventh facility, a decommissioned underground control bunker from a nuclear missile defense system located near Albion, France, is deployed to sniff out alpha contamination problems prior to production release, according to Lesea.

To Xilinx, Astep's lab is "only one of three accelerated sites," Lesea said, adding, "We are still evaluating its usefulness."

Tezzaron's Patti said his company "might be interested" in what Astep has to offer but added that he is uncertain whether real-time SER testing in high altitude will yield timely data. "I would need to see what ST and Xilinx have learned," he said. "I need convincing."

NXP's Heijmen said he's hopeful that ST will share Astep results with Crolles2 Alliance partners NXP and Freescale. Under the Crolles2 agreement, the three partners work closely together on SER estimations of their shared intellectual property. Heijmen noted the Astep lab's dedicated system "allows the testing of hundreds of chips for weeks or months."

According to Derbey, iRoC earlier agreed to take part in Astep. But the final signing is still "pending," he said, noting that Astep must secure investments for extra buildings and more equipment before becoming a full-fledged SER testing site.

"There's still huge work that still needs to be done" at Astep, Derbey said. But he hopes the Astep initiative will bring "significant value as it aggregates industrial testing and research activities."