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Samsung puts charge in NAND at 40 nm

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Taipei, Taiwan -- Looking to snatch back its mantle as NAND flash leader, Samsung Semiconductor trotted out a 32-Gbit chip made on 40-nanometer process technology last week that eliminates the traditional floating-gate structure. Instead, it sports a proprietary oxide-nitride-oxide layer that the company calls charge trap flash.

Samsung also introduced its latest phase-change memory prototype, with a density of 512 Mbits.

The NAND development comes just months after IM Flash Technologies LLC, a joint venture of Intel Corp. and Micron Technology Inc., one-upped Samsung by sampling a 4-Gbit NAND flash memory in a 50-nm process. IMFT released the chip just days after Samsung said it was mass-producing flash using 60-nm technology.

Samsung now claims its charge trap flash (CTF) technology will allow it to more easily scale NAND down to 30 nm and even 20 nm--which would yield a 256-Gbit chip. This could possibly give the company an edge over competitors if they are unable to scale traditional floating-gate technology. IMFT showed some unique techniques in achieving a 4F2 cell factor in its 50-nm device, however, and some analysts think NAND will scale for a few more generations.

Samsung declined requests for more in-depth technical details of the development, but said in statements that a CTF-based NAND chip would be more reliable because it reduces cell-to-cell interference that can make the bits harder to read. CTF-based NAND eliminates the floating gate, a key component of traditional NAND, and instead traps the charge in the nonconductive silicon-nitride layer that's sandwiched between two layers of oxide. Samsung believes that this approach increases reliability and control of the storage current.

Samsung refers to the total structure as Tanos, which comprises tantalum (a metal), aluminum oxide (a high-k material), nitride, oxide and silicon layers. Using a Tanos structure marks the first application of a metal layer coupled with a high-k material in a NAND device, Samsung said.

Samsung's approach seems similar to the path Spansion Inc. took for its MirrorBit NOR. MirrorBit technology also uses a trapped-charge, nitride-based architecture and eliminates the floating gate. Spansion claims that doing so means one fewer poly layer, which translates into a 40 percent reduction in masking steps and yield improvements as high as 30 percent compared with multilevel-cell floating-gate technology. Samsung believes it can reduce process steps by 20 percent and cell size by 28 percent.

"All of these improvements look good on paper," said Geoffrey MacGillivray, an analyst at

Semiconductor Insights, which provides technical and patent analysis of ICs. "However, 40 nm is very aggressive, so we're interested to see how Samsung has implemented them in this device."

Interestingly, Samsung's ability to aggressively push NAND to 40 nm "bodes badly" for the near-term commercialization of other new nonvolatile memory technologies, such as PRAM, FRAM and MRAM, said Jim Handy, director of Nonvolatile Memory Services at Semico Research Corp. "Alternative technologies will make most sense once flash reaches that brick wall where it can no longer migrate to the next smaller process node," he said.

Magnetic random access memory and ferroelectric RAM are just being slowly introduced into the market. During the last few years, such companies as Intel, Renesas, Elpida, STMicroelectronics, Sony and Toshiba have also stepped up their efforts on phase-change memory, also known as PRAM, PCM and Ovonic Unified Memory. Since 2004, Samsung has introduced 64-Mbit and 256-Mbit PRAMs, and late last year it licensed PRAM technology from Ovonyx, an early developer of phase-change memory.

PRAM is a phase-change memory that is similar to the technology used in CDs and CD drives. Both leverage the distinct behavior of chalcogenide glass, but in different ways. In a PRAM, an electrical current heats a chalcogenide film to either a crystalline or amorphous state, which have very different electrical resistivity. This allows the two states to be read as a 0 or 1.

Among all the companies developing PRAM, Samsung has a huge in-house application--cell phones--in which it could be very useful, if the technology holds up as a universal replacement memory. "If you look at Samsung's current offering for 3G [third-generation] cell phone memory," said Bob Merritt, who covers emerging memory technologies at Semico, "you can see a multichip package with two DRAM die, two PSRAM die, two NAND die and two NOR die. So it is obvious that the memory technologies developed for box-level computing applications are just not the most efficient memory technologies for these highly mobile applications.

"However, the performance range of some of the developing new memory technologies--and specifically the performance range of phase-change memories--can neatly fit into that 3G application and can ideally become eventually embedded into the processor die itself," he said.

Samsung said its PRAM will be competitive against NOR flash when it becomes commercially available in 2008. Applying vertical diodes to form the 3-D transistor structure used in its DRAM process, engineers were able to achieve a 0.0467-micron² cell size, the smallest thus far and only half that of NOR. Samsung did not provide details on which NOR chips it used for comparison, nor did it reveal the programming current necessary to effect the phase change. Samsung used a 400-microamp programming current in a 256-Mbit array last September. A few months later, Renesas said it used 100 μ A to program a 1.5-volt PRAM.

One of the last hurdles for PRAM will be cost per bit, said Mark DeVoss, a senior analyst of flash and emerging memory technologies at iSuppli Corp. "At this point, PRAM is not competitive with existing memory types, but it has the attribute of high speed, ultimately a competitive cost per bit and nonvolatility. I would suspect it could cannibalize the slow SRAM, followed by the NOR flash business . . . but will have a greater challenge displacing high-speed SRAM, DRAM and NAND flash," he said.

Samsung said its first high-density part will be the 512-Mbit device.



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