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Flash design preps for high-end cell phone battle

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Austin, Texas — In a counterattack against NAND memory vendors moving onto its cell phone turf, Spansion LLC will begin sampling a newly architected MirrorBit flash that is pin-to-pin compatible with NAND flash memories.

The memory architecture, named Ornard, includes parallel banks of NOR-type flash, with a NAND interface. In a presentation at the company's Fab 25 here, CEO Bertrand Cambou said the structure improves on the relatively poor write speeds seen in typical NOR devices, with burst-write speeds that are four times faster than NAND chips.

"NOR is slow at programming and writing. NAND is slow to read. With Ornard, we believe we have picked the best of each, for the ultimate reliable solution for multimedia systems," Cambou said.

The device family will sample at hefty 1-Gbit densities, using Spansion's newly qualified 90-nanometer process at Fab 25.

Ed Keyes, chief technology officer at Semiconductor Insights Inc. (Kanata, Ontario), said Spansion executives "see Ornard as their NAND killer in the high-density cell phone market. That is where NAND is starting to nibble at the high-density NOR." Just as a pseudo-RAM is a DRAM configured to look like an SRAM, the Ornard is a NOR device that works like a NAND chip, he said.

While the design does not support XIP (execute in place), Ornard is designed for applications that either use a separate NOR device for XIP, or in systems in which code is shadowed from an Ornard into an SDRAM memory, the "store and download" mode that, according to some market researchers, is gaining traction against the XIP mode.

With an ability to store both code and data, Ornard will enable Spansion to "participate in the part of the NAND market that is the highest-price niche," said Jim Handy, a Semico Research analyst.

Ornard "probably will find its niche," Handy said.

Spansion — which is a joint venture owned by Advanced Micro Devices Inc. and Fujitsu Ltd. — is coming out with the product at a time when it's preparing to make an initial public offering en route to becoming an independent company.

Spansion had \$2.4 billion in revenue last year.

After the presentation, Spansion's vice president of system engineering, Robert France, demonstrated a board-level mockup of a video-capable cell phone that used Ornard flash to buffer video directly into a Texas Instruments Inc. Omap applications processor, at 15 frames per second. On a separate daughterboard, a NOR device was stacked in a multichip package with the baseband processor.

France said Ornard is optimized for handling MPEG-4 video and for rapid-fire digital images in "multishot" cameras within high-end cellular phones. Other applications may include car navigation systems and video cameras, and in the handheld dictionaries popular in the Far East for translating words from Asian languages into English.

Ornand memories will have higher reliability than NAND devices, Cambou asserted, due to less stress on the oxide layer during programming.

Phone makers are reluctant to use NAND architectures for storage of critical code because a phone can go dead if bits are corrupted. To program and erase, NAND memories use Fowler-Nordheim tunneling, while MirrorBit devices employ hot carrier electrons.

Cambou said NAND's susceptibility to drop bits requires error correction circuitry (ECC) on NAND while NOR devices are reliable without ECC.

Also, while NAND usually shines in terms of density, Cambou said Ornand's die size is 81 square millimeters for the gigabit part made in a 90-nm process. Samsung, he said, requires 80 mm² for its single-level-cell gigabit-density NAND.

A Samsung spokesman said it has not placed any multilevel-cell (MLC) parts on the market thus far. That will change soon, as it begins ramping a 4-Gbit MLC part aimed at digital audio and other markets.

Also in the fourth quarter, Spansion intends to sample gigabit-density NOR devices. While the gigabit-density Ornand will operate at the 1.8 volts required for cell phone acceptance, the gigabit NOR devices will start out at 3-V operation, a spokeswoman said.

Spansion has based its newest products on its MirrorBit technology, in which two bits are stored in a nitride layer within the bit cell. MirrorBit differs from the multilevel-cell approach taken by Intel Corp. and others, in which four voltage levels represent two bits in a single cell.

Cambou said the Spansion research lab in Sunnyvale, Calif., the Submicron Development Center, is making progress on combining the two-bit MirrorBit technology with an MLC voltage scheme that would deliver four bits per cell.

With Spansion on track to make gigabit MirrorBit parts early next year in volumes, Jim Doran, executive vice president of operations, said two-thirds of Spansion's overall capacity soon will be dedicated to MirrorBit two-bit-per-cell products. By mid-2006, the company will make a "hard switch" to 90 nm, turning off its older 110-nm process at Fab 25 and switching to the 90-nm process. To that end, Spansion recently signed a foundry agreement with Taiwan Semiconductor Manufacturing Co. Ltd. to produce Spansion products at 110-nm design rules, allowing Fab 25 here to move faster to 90-nm design rules.

Augmenting its existing three fabs in Japan, Spansion is building a 300-mm line in the Aizu region of northeastern Japan that will be dedicated to 65-nm production. The Austin fab will be Spansion's only 90-nm fab, using 200-mm wafers, said Doran.

Doran said microprocessor vendors bring out a new process with an emphasis on switching speed. A new flash process must accommodate the charge pumps required to send 10 to 12 volts during programming.

"These high-voltage transitions at the 90-nm node are a challenge. And we have to guarantee that once we put the charge there, that it will stay there for 20 years. Durability and reliability are big challenges in flash manufacturing," said Doran.

Meanwhile, Intel has been shipping single-level-cell NOR devices made with its 90-nm process since the first quarter, an Intel spokeswoman said. Though one financial analyst recently speculated that Intel's MLC parts on 90 nm were delayed, the spokeswoman last week said that Intel "is on track" to produce a 90-nm MLC flash chip by the second half of this year. Code-named Sibley, the 90-nm MLC

flash technology will start out at the 512-Mbit density, with two of those chips offered in a stacked package for customers that seek gigabit-density products.

Moreover, Intel engineers have boosted performance, creating zero-wait-state parts that run XIP code at 1 MHz, with 500 kbytes/second of write speed.

Denying arguments that NAND parts would displace NOR in the cell phone market, the Intel spokeswoman said that with NOR devices, "XIP code and data can be stored on the same chip, alleviating the extra RAM. That is why we have worked to increase the read and write speeds for NOR."

Taking a different approach to the cell phone memory market, Samsung Semiconductor is marketing its OneNAND flash part to cell phone manufacturers, arguing that a modified NAND is the most cost-effective choice for data-intensive phones. Dan Barnetson, associate director of flash marketing at Samsung, acknowledged that NAND devices do suffer from bad bits over their lifetime, but he said NAND vendors have developed system-level recovery methods that guarantee error correction and bad-block recovery.

"The problem with NOR is that by our calculations 1 to 3 percent of the NOR bits expire over the overall lifetime of the part, but with NOR devices the system has no way to recover," said Barnetson. At the upcoming Denali MemCon conference in Silicon Valley, Samsung will present new system-level recovery techniques for NAND, comparing that with NOR-based systems, he added.

"With OneNAND, we can stream HDTV-level video to a portable system at 10 Mbytes/s. That can shorten the download time significantly compared with NOR, resulting in much longer battery life," he said, adding that NAND devices conserve on power by programming many bits in parallel.

Samsung will move to a 73-nm process starting next year, upping its OneNAND density to 2 Gbits from the current offerings ranging from 128 Mbits to 1 Gbit.

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