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## New memory materials will enable future 'untethered' electronics

*Growing uneasiness over the ability to continue shrinking existing CMOS memory cells and the push toward portable electronics are helping to foster R&D on new memory technologies.*

There are two very different reasons for the interest in new memory devices. The first is growing concern over the ability to continue shrinking existing CMOS memory cells of dynamic random-access memory (DRAM), static RAM (SRAM), and flash. All of these devices retain information by storing charge in structures that consist of capacitors and transistors. As these structures shrink, the surface area available for capacitors is reduced, and the increasingly complex challenge of providing enough mass to store the charge is a concern for memory manufacturers. For SRAMs, the challenge is dealing with the growing probability of soft errors. Flash devices have their own impediments to storing multiple bits in each cell.

The rate of progress may be tightly coupled to advances in lithography. Regardless of whether a new memory technology is based on magnetic properties, changes of resistance, or even the up/down position of nanotubes, the ultimate impact of the technology on DRAM, SRAM, and flash products will be governed by the ability to make smaller lines and cells.

There is a flaw, however, in assuming that the value of new memory materials is ultimately controlled by advances in lithography and Moore's law. This masks the true impact of new memory technologies. While the predictability of lithographic advances may affect the extendibility of DRAM or flash, the implications of new memory materials go beyond the usual objectives of faster/smaller/cheaper. Successfully achieving the design goals driving magnetoresistive RAM (MRAM), ferroelectric RAM (FeRAM), ovonic unified memory (OUM), programmable metallization cells (PMC), and other new technologies will result in drastic direction changes for semiconductor companies and will lead to unique processor architectures.

The second reason for high interest is the push toward portable electronics. In the early days of semiconductor production, Intel, Motorola, Texas Instruments, Mostek, and other companies were the leading memory manufacturers. At that time, fabrication facilities were expected to manufacture a wide variety of products. Logic and memory products were often fabricated in the same facility, albeit with certain changes in the manufacturing flow.

During the 64K DRAM product cycle, Japanese companies proposed a radical strategy of dedicating large facilities to producing only memory products, with the focus on DRAMs. The theory was that dedicated facilities could achieve lower manufacturing costs and higher yields than general-purpose facilities. The trade-off was that memory designs would have to minimize the logic on the die. The move represented a fundamental shift in manufacturing strategies, and was predicated on the growing demand for large memory arrays.

With the support of computer OEMs, standards organizations supported the new manufacturing strategy. That split between memory and logic processes continues today. The steep decline in the cost/bit of commodity memory served the market well as OEM products migrated from mainframes to minicomputers and, finally, to PCs. Architectures that continue to combine memory and logic now fall into the specialty domain of "embedded memory."

As the growth of desktop PCs has slowed, the driving force for new technologies has shifted toward smaller architectures. Nick Tredennick, editor of the *Gilder Technology Report*, differentiates between tethered devices that remain attached to their power and data sources, and untethered devices that carry their own storage media and power sources. The impetus for many semiconductor technologies has become the smaller form factors of untethered devices. One obvious embodiment of this new focus is the cellular handset.

Emerging 3G cell-phone technologies create severe design challenges, due to the simultaneous transition to newer and more complex protocols while adding more features. The fact that we cannot increase the size of the phone while substantially reducing power requirements is a design constraint. We want something that is battery-powered with multimedia functionality and that can operate in a very dynamic environment. And we want it to remain in its current form. The diagram on page S25 shows a typical cell phone architecture.

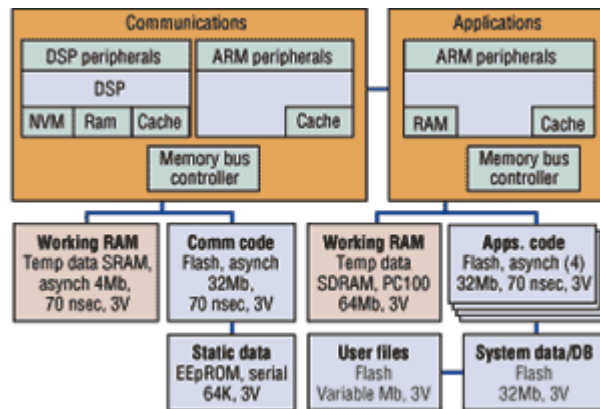


Diagram of typical cell phone architecture. (Source: Intel, Spring IDF 2002)

In the quest to reduce the size and power of handsets, it is critical that the number of components be reduced. The elusive goal of a single-chip cell phone is still beyond reach. At the moment, much of the attention is on stacking more die in a single package. Eventually the total number of die needs to be reduced, and this means that the memory must move onto the same die as the processor.

Most major companies are pursuing the development of memory technologies that will be compatible with logic processes. TI hopes to integrate FeRAM memory into its designs, Motorola is focused on MRAM, and Intel is concentrating on OUM. The objective of all three companies is to find a high-performance nonvolatile memory technology that can be combined with their respective logic processes.

### New memory materials

The table identifies some of the publicly announced memory programs and the companies that contribute that particular intellectual property (IP). These research efforts can be restated with different emphasis and a very different implication. The essence of these programs is not about finding the replacement for cost-sensitive DRAMs, or about extending lithographic boundaries and adhering to Moore's law for another decade; it is about enabling a fundamental shift in semiconductor manufacturing flow away from PCs and toward battery-powered untethered devices.

Major contributors of memory IP				
Common name	Description	IP contributors	Activation event	Measured by changes in:
MRAM	Magnetic random access memory	IBM, Honeywell, Motorola, NVE	Electric current switches magnetic polarity of the cell	Resistance
FeRAM	Ferroelectric random access memory	Ramtron, Symetrix, TI	Voltage polarizes dipole structures within cell structure	Capacitance
OUM	Ovonic unified memory	Energy Conversion Devices, Ovonyx, Intel, ST Microelectronics	Electric energy generates heat that converts material between crystalline conductive and amorphous resistive phases	Resistance
Ion flow	Programmable metalization cell (PMC), NanoBridge	Arizona State U., Axon, NEC, Infineon	Ion flow creates a reversible nonvolatile path of low or high resistance in solid material	Resistance
Polymer	Polymer memory	UCLA, Russian Academy of Sciences, Coaltue, IBM, Infineon	Ion flow creates a reversible nonvolatile path of low or high resistance in plastic material	Resistance

As dramatic as these opportunities may be, there is an even larger potential. With this much memory available in the die on the plane above the logic, the architecture of the processor can be changed to take advantage of this on-chip high-performance memory. Several examples of merging logic and memory are already available. Companies such as Xilinx and Altera utilize embedded SRAM to structure temporary logic gates for field-programmable gate arrays (FPGA). These devices can be reprogrammed quickly and an almost infinite number of times, but the information is lost when the device is powered down. On the other hand, complex programmable logic devices (CPLD) use an embedded nonvolatile memory technology. Data can be retained up to 20 years, with limited read/write cycles.

Adaptive computing processors, based on embedded SRAM, show a more complex usage of memory and logic. The hardware associated with the data routing and logic structures is reconfigured for each new task. Performance thus can be optimized over a wider variety of tasks than a traditional general-purpose processor. This is critical to meeting the needs of data communications and cell phone applications, with constantly evolving protocols and standards. The impact of the memory on processor cost and performance is that SRAM cells occupy up to 60% of the entire die.

Researchers from NEC and NIMS released a paper that expresses the full impact of the technology at this year's International Solid-State Circuits Conference (ISSCC): "One of the promising applications of the switch is in field programmable devices...Substituting a solid-electrolyte switch for the SRAM-based one leads to two important advantages. First, the size of the proposed switch is reduced...Moreover, because the switch is stacked in the logic cells, the cell occupancy is increased even more. Second, the ON resistance is so low ( $<100\Omega$ ) that the signal delay can be minimized" [1]. Thus the paper presents a low-power, fast, dense, nonvolatile memory cell that is compatible with a logic process and can be stacked on top of the logic cells.

## Conclusion

The goal of being able to communicate anytime and anywhere reflects that untethered devices are one of the objectives of new semiconductor technologies. A critical requirement for future advances of these devices is compatibility with logic processes. Whether this research and development falls under the heading of cell-phone memories or nanometer switches, the impact of these programs will go far beyond the memory cells!

## Acknowledgment

OUM is a trademark of Ovonyx Inc.

## Reference

1. T. Sakamoto, S. Kaeriyama, H. Sunamura, M. Mizuno, H. Kawaura, et al., "A Non-volatile Programmable Solid-Electrolyte Nanometer Switch," presented at ISSCC, paper 16.3, Feb. 2004.

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