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## Bright Future Expected For Configurable Processors

**Speakers at ARC International's ConfigCon Silicon Valley conference said configurable processors have many opportunities and predicted a strong growth curve.**

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SANTA CLARA, Calif. — Configurable processor cores are on a rapid growth curve and have "great opportunities" in many embedded applications, said analyst Jim Feldhan, keynote speaker at the ConfigCon Silicon Valley 2006 conference here Monday (Oct. 30). Other speakers also described a bright future for configurable processors.

[ConfigCon](#), which has been held in Taiwan and China but is appearing for the first time in Silicon Valley, is sponsored by [ARC International](#). Presenters included representatives of EDA vendors, real-time operating system (RTOS) providers, silicon intellectual property (IP) suppliers, and foundries.

Feldhan, president and founder of Semico Research Corp., said that total processor cores account for around 2.5 billion units today and will approach 4 billion units by 2010. Configurable processors account for 200 million units today and will reach 1 billion units by 2010 — a much faster overall growth curve than non-configurable cores, Feldhan said.

"There's a great deal of design work going on right now, and there's a great opportunity for ARC, Tensilica and other vendors as well," Feldhan said. Good opportunities for configurable cores, he said, include markets with new standards that are in flux; applications that require the processing of a large amount of data in a limited time; and power management for portability, where reducing clock cycles is important.

Feldhan said that configurable cores should do well in applications such as wireless networks, multimedia, streaming video, image processing, HDTV, and old and new portables. He said that configurable cores provide product differentiation, address multiple standards, support multicore designs, and protect designers' IP.

Feldhan also reiterated a [previous Semico forecast](#) that predicts a short downturn in semiconductor industry growth in 2007, followed by strong market growth through 2010.

Meanwhile, speakers from ARC presented configurable processors as a new chip design methodology for the 21st century. "We believe this represents the future of SoC [system on chip] design," said Carl Schlachte, ARC president and CEO.

Schlachte said that Moore's Law actually inhibits the creation of low-cost SoCs, because increasing complexity results in high design costs. "We need to be able to utilize SoCs without touching every transistor," he said. "The IP industry was born on the back of this fact."

But there are problems with legacy, "fixed" IP architectures, Schlachte said. One, he said, is that fixed processors "at their heart restrict innovation," because users have to adhere to a standard. Schlachte also

argued that 20th century CPUs are not suited for low-cost embedded applications, and that hard-wired logic doesn't adapt to changing protocols.

"Configurability offers SoC designers the freedom to create highly differentiated chips that provide a competitive advantage," Schlachte said. Configurable CPUs, he argued, have lower power consumption, require fewer transistors, and are less expensive to manufacture.

Schlachte noted that ARC was one of the pioneers of configurable processors, and is now moving towards configurable subsystems for audio and video applications. An example is the [ARC Player Subsystem](#), which includes a 32-bit ARC 600 family core with media extensions, MPEG-4 video decoder, MP3 decoder, audio/video synchronization, and a voice recorder module.

Nigel Topham, chief architect at ARC, provided more detail about the "benefits" of configurability. By adding a small number of additional, application-specific instructions, he said, users can experience significant speed gains, code size reductions, and increased energy efficiency, all with a "small increase" in die size.

Configurable custom logic can also replace lookup tables, he said. While a lookup table can require 100 clock cycles to decode a symbol, a configurable processor can reduce this time to one clock cycle, Topham claimed. He also said configurable custom logic can provide 20X better energy efficiency, improved cache performance, and a reduced memory bandwidth.

Multimedia SoCs will require a massive growth in complexity, but clock frequencies will not rise significantly, Topham said. Thus, multi-core parallelism is essential, and this requires configurability in terms of the number and connectivity of cores. Thus, he said, platform architectures will become configurable multi-core architectures.

Topham briefly described the VRaptor Media Architecture, introduced [earlier in October](#), which supports an ARC 700 family core with a single-instruction, multiple-data (SIMD) accelerator and DMA engine.

After his talk, Topham's claim about energy efficiency was challenged by an audience member who noted the increasing problem with leakage power. "There is no single answer to the problem of leakage power," Topham said. "But we think configurability allows us to produce a solution that is inherently more power efficient."