



Inapac Technology Releases New DRAM IP Designs Optimized for System-in-Package (SiP) Applications

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SiPFLOW(TM) Platform Enables Low-Cost, Reliable SiPs for Media-Rich Applications
SAN JOSE, CA -- (MARKET WIRE) -- 11/10/2005 -- Inapac Technology, Inc., a provider of intellectual property (IP) and services to ensure reliable system-in-package (SiP) memory integration, today announced the release of two designs. The new 32M-bit SDRAM and 64M-bit DDR (Double Data Rate RAM) designs expand Inapac's SiPFLOW™ platform, which provides a low-cost infrastructure and exceptional levels of production quality and reliability for manufacturers of SiPs for such media-rich applications as cell phone media processors and LCD display controllers. The 64M-bit DDR design is the industry's first such implementation for low-power/high-performance applications to feature a x32 interface, which is critical for superior graphics and video performance in consumer applications.

The Inapac SiPFLOW platform includes a family of memory IP designs, a proven testing infrastructure, and specialized SiP testing services and support. The IP designs are optimized for SiP integration, including small footprint, low power consumption, and high-bandwidth operation via a wide bus interface. They also incorporate the Inapac VIBE™ (Voltage-Induced Burn-in Emulation) and SiPLINK™ test technologies, which support economical wafer-level test and screening and "in-system" memory test within the finished SiP device. Proven in high-volume manufacturing on a 0.14μ process with Inapac's DRAM foundry partner, the designs and full test methodology support are available now for licensing and production ramp.

"Experience with our first design, a 16M-bit SDRAM that has already been implemented in high-volume production, has shown that the SiPFLOW platform can deliver exceptional, less-than-200 dppm reliability at low cost," said Naresh Baliga, vice president of marketing for Inapac Technology. "With this proven methodology, we're expanding the range of our licensable designs to offer the density and speed grades needed to meet a broader range of SiP design requirements."

SiP-Optimized Memory Design

The Inapac SiPFlow platform was developed to address the challenges of ensuring the quality of separate, KGD (known good die) components and achieving consistent, reliable system assembly. To support these goals, the DRAM designs integrate a unique and proprietary test bus that allows for full test without burn-in, as well as testing of the finished SiP.

This design-for-test architecture and methodology is a two-step process. Wafer-level test uses the Inapac VIBE methodology, which is equivalent to traditional oven-based burn-in testing without the capital-intensive operational infrastructure. After SiP assembly, the memory portion of the SiP is tested using the SiPLINK test gateway, utilizing industry-standard test equipment to verify functionality, allowing the SiP integrator to screen out additional quality-related issues that may have been introduced as a result of the SiP assembly steps.

Configuration, Availability

Inapac DRAM designs are available in different speed and power versions and in x32 and x16 bus widths, to suit specific application needs. These include mobile phones with such advanced multimedia features as video and still camera, music and gaming, as well as high-resolution LCD video displays for desktop and portable computers and digital TVs. They can be used for SiP implementations in stacked (die-to-die) or side-by-side (die-to-substrate) configurations in all typical SiP package types (BGA, QFP, etc.). The new 32M-bit designs, available in 200 MHz at 2.5/3.3V or

133 MHz at 1.8V versions, are fully characterized for production. The 64M-bit designs, available in 250 MHz at 2.5V or 133 MHz at 1.8V versions, are sampling now.

About Inapac

Inapac Technology, Inc. is a leading provider of technology and services for system-in-package (SiP) applications, focused on providing IP to enable the production of reliable, cost-effective memories optimized for SiP. Products based on the company's patented SiPFLOW™ platform are licensed to semiconductor and systems companies to enhance the performance, quality and reliability of products in the cell phone, consumer audio/video, digital imaging, and storage markets. Inapac is headquartered in San Jose, California, with additional offices in Boise, Idaho, and Hsinchu, Taiwan. For more information, visit the company's website at www.inapac.com.

EDITORS NOTE: The following industry analysts have been briefed on Inapac Technology and are available for comment:

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