

NEWS & TRENDS

Panelists ponder challenges of 45nm

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The move to the 45nm process node will be costly and challenging, but worth it for selected applications, according to panelists at the EDA Tech Forum here Thursday (Nov. 3). Moderated by Wally Rhines, Mentor Graphics CEO, the panel was entitled "The road to 45nm, a highway to hell?" But that wasn't the panel's conclusion. Despite steep design and fabrication costs, panelists were generally optimistic about the ability of EDA and foundry providers to come up with solutions, and of designers to leverage their investments in 45nm technology through intellectual property (IP) reuse.

Jim Feldhan, president of Semico Research Corp., said there's a "short list" of potential products that will need 45nm technology during its first few years. These include microprocessors, high-end graphics, memories, and any applications that need the transistor count and can drive high volumes. But with fabs costing perhaps \$6 billion, he said, only a handful of companies will be able to build 45nm fabs.

By 2012 or so, he said, 45nm technology will be mature enough, and have enough design tool support, to attract a broader range of applications.

If there's an improvement in cost per function, "good things will happen at 45nm," said John Martin, vice president for strategic alliances and partners at Chartered Semiconductor. But it's not cheap. He acknowledged that \$2 million mask costs are "not out of the question," and said the major investment will be in the up-front design effort.

Ted Vucurevich, Cadence Design Systems CTO, agreed that 45nm design costs will be very high. Because of issues like variability, verification, and growing software content, he said the cost of the "first gates" at 45nm will be higher than at 65nm. But Vucurevich said that designers will be able to leverage their investments through reusable architectures and IP, thus amortizing the cost across multiple products.

Vucurevich also said he is "very bullish" about the 45nm mode opening up new opportunities for EDA vendors. In addition to design for manufacturability, he said that new tools will be needed for architectural design and verification.

The costs of 45nm will raise the stakes, noted Martin. "To be successful, you have to be relatively certain of first pass success," he said. "This can be achieved through the diligent efforts of everyone in the tool chain."

Andrew Kahng, chairman and CTO of Blaze DFM, said that the "business organization" of EDA vendors hampers the development of solutions. He said the challenges of 45nm design include density, leakage, and return on investment. Another challenge, he said, is "the aging mindsets like design rule manuals, or SP&R [synthesis, placement and routing] handoff to manufacturing. Those are really showing stress at 65nm and probably won't survive the transition to 45nm."

Kahng noted that manufacturing variability may cause excessive guardbanding and uncertainty. "We need to design around variability and understand what is easily modeled," he said. "We need to find systematic variation and pull it out and get rid of excessive guardbanding."

New transistors may also come into play at 45nm, Martin noted. "There's an enormous effort with all kinds of new devices, and it's difficult to predict which one will supplant planar transistors. The vote is still open," he said.

Rhines asked panelists when the industry will move to statistical methods to combat variability. "1979," replied Vucurevich. "As an old analog designer I'm laughing. Digital guys have come up with ways to hide all that stuff, but advanced design teams have been dealing with these issues since the 130nm node. The real question is when we need to democratize the [statistical] technology for the rest of the design community. I think the answer is now."

EDA Tech Forums are held at various locations throughout the year. While sponsored by Mentor Graphics, the events are not restricted to Mentor customers.

- Richard Goering
EE Times

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