



### **SOI cheaper than bulk CMOS, according to Semico study**

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When delving into the total cost of producing performance devices that operate at lower power consumption levels, silicon-on-insulator (SOI) substrates can result in as much as a 40 percent reduction in the overall cost of doing so, compared to conventional bulk CMOS design, process and packaging methods.

This is the conclusion from a Semico Research Corp in-depth study on the actual impact of SOI wafers on the cost of operation, the cost of manufacturing and the ultimate cost of the end product.

"On a straight manufacturing cost basis, the 10-15% SOI cost-of-ownership (COO) figure does not tell the whole story," said Joanne Itow, Managing Director of Manufacturing at Semico. "Moving further into the semiconductor manufacturing process, looking at the cost of SOI once the wafer is tested, diced and the good die packaged, the Semico analysis has found the SOI COO adds only 4-6% to the total manufacturing cost."

A key factor noted in the study by Itow was that SOI produced devices had an advantage in being able to support less on-die memory than bulk silicon devices, which is consuming an ever-increasing portion of a microprocessor die real estate, resulting in little actual die shrinkage node on node.

"Use of SOI-enabled memory optimization tools can increase the benefits of SOI from breakeven to a cost reduction of over 40%, depending on the product, technology and process complexity," concluded Itow.

Soitec the major producer of SOI wafers for advanced semiconductor applications has seen demand increase significantly in recent years and now plans to build its third manufacturing plant to cope with demand. AMD, IBM, Chartered Semiconductor and Sony are all major customers that are ramping microprocessor production at the 90nm node primarily on 300mm wafers.