

Advanced memories still struggle in mobiles

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Don't ask M-Systems CTO Meir Avraham about the so-called universal memory. He doesn't buy the idea that a single memory will meet all the needs of tomorrow's portable systems.

According to the former Israeli Defense Ministry researcher, each new memory type has its strengths and weaknesses, mandating a detailed understanding of each. Phase-change memory may challenge floating-gate NOR flash if it can overcome power consumption challenges. But it won't match NAND on cost. MRAMs have a chance to replace SRAMs in certain applications, but their cell size and power consumption are larger than that of NAND flash.

"I don't believe the industry will ever find the ultimate, universal memory," Avraham said. "I think that is a dream that engineers like to talk about."

Indeed, memory research managers themselves have scaled back their rhetoric in the past, avoiding the term universal memory altogether. After a period of exaggerated claims, companies became so quiet about any progress that analysts speculated efforts had been severely scaled back in ferroelectric (FRAM), magnetoresistive (MRAM) and phase-change (PRAM) development.

But managers at Freescale Semiconductor Inc., Intel Corp. and Texas Instruments insist that those programs are alive and kicking, even as they acknowledge that the road is long and uphill for any new memory type.

Ageing incumbents

The three memory technology incumbents—DRAM, EEPROM/flash and SRAM—have dominated the industry for three decades and more, and all are showing their age. DRAM capacitors have become preternaturally tall and skinny; flash, to extend the poly-to-poly dielectric, must tap a high-k material; and SRAMs face SNR and soft-error-rate challenges as scaling proceeds.

Bob Merritt, DRAM analyst at Semico Research, noted that the portable-systems industry is riding the multichip-package (MCP) wave. Samsung Semiconductor's latest MCP stacks flash, DRAM and SRAM dice eight high. But Merritt argues that MCPs are less than ideal in terms of power consumption, thermal issues and bandwidth. "Eventually, I think the industry will find something that is superior to today's memories in terms of power consumption," he said. "If you look at what Intel, TI, IBM and Freescale are working on, all can be embedded memories that are compatible with CMOS logic."

Saied Tehrani, director of MRAM technology, said Freescale demonstrated a 90nm MRAM with an aluminum oxide tunneling layer. The demo showed that the 180nm cell could be shrunk to 2.9 2 in a 90nm logic process, which includes low-k dielectrics. Now, the Freescale MRAM group is replacing aluminum oxide with magnesium, which will reportedly improve the bit resistance and allow the tunneling layer to be thinned slightly.

With aluminum oxide in the magnetic tunnel junction, MRAMs undergo a 30 percent resistance change as the bit changes from zero to one. With magnesium oxide, that resistance change can be 90 percent to 100 percent, with huge implications for MRAM technology.

"Some companies came in with huge expectations that didn't materialize fast enough for them," Tehrani said. "I believe MRAM technology still has a lot of promise, and we are seeing that at Freescale. It still is a challenge getting the cost structure and the volumes to the point where it can have a huge impact on giant markets. That is the challenge with any new memory technology."

Hiroaki Yoda, a manager at Toshiba Corp.'s advanced-memory technology department, said the main challenge still facing MRAM is the large programming current. But Yoda said MRAM technology is making rapid progress, citing "great advances" with the introduction of magnesium oxide barriers and spin momentum transfer technologies.

As a result, "nanosecond read speeds are possible and the objective of reducing programming current has become a little more realistic. This is completely different from other emerging memory technology development efforts, in which no big innovations have been made," Yoda said.

PRAM meets internal targets

Greg Atwood, Intel Fellow for non-volatile memory technology, said that Intel is beefing up its phase-change memory development effort. The Intel program is "increasing, although we tend to be pretty quiet about it. We continue to see good results," Atwood said. Intel also went through its ups and downs, trumpeting the effort in the early stage and then acknowledging that phase-change technology faced cost challenges. The strong suit of phase-change memory, Atwood said, is its ease of scalability.

Today's memories are all charge-storage types, and all are approaching fundamental physical limitations. As companies try new materials to compensate, the memories' complexity increases with diminishing returns on the effort expended.

Ted Moise, director of the FRAM development group at TI, said that TI remains confident about its FRAM co-development effort with Ramtron International. TI had planned to have a 90nm FRAM process ready last year, but then stepped back to a 130nm process.

At the outset of its program, TI had to build up an infrastructure, which required new materials and equipment programs, and new test and reliability methodologies. "Creating all that from scratch takes time, but we've made great progress and have several products that will be very useful to TI's customers," Moise said.

The beauty of FRAM for TI's product portfolio is the "ultralow power" consumption, Moise added. "In the low-power embedded space, FRAM is very competitive. It is also logic-library-compatible. For embedded flash, the high voltages required to program the transistors become more of an issue; the voltages are so disparate between the flash and the logic. And the cells are about one-third the size of SRAM," he said.

Last year, TI gained manufacturing experience by making a discrete 4Mbit FRAM, co-developed with Ramtron, at one of its Dallas fabs. The partners will make an 8Mbit FRAM design presented at last year's Custom Integrated Circuits Conference.

After making the discrete parts, TI will use FRAM for chipsets. Moise was reluctant to say which chipsets would see first use, but said the company will work up to the high volumes within the cellphone sector.

- David Lammers
EE Times

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