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IntellaSys Unveils Revolutionary "Scalable Embedded Array(TM) (SEA) Platform" to Launch Multicore Processor Chip Solutions

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CUPERTINO, Calif.--(BUSINESS WIRE)--May 15, 2006--Inaugural SEAForth(TM) Chip Family Promises to Raise Performance-Per-Watt Bar in Embedded Applications That Need to Operate at High Speed and Low Power.

IntellaSys Corporation today formally unveiled its Scalable Embedded Array(TM) (SEA) Platform to launch multicore processor solutions for next-generation embedded applications. The performance-per-watt benefits of the revolutionary platform are evident in the inaugural SEAForth(TM) product family, which was also formally introduced with its first entry, the SEAForth-24 chip solution. Packing 24 core processors, each of which can operate at one billion instructions per second, the SEAForth-24 chip dissipates only 150mW in a typical application.

"Our launch today represents a major milestone in embedded multicore processor design and the culmination of more than 200 man-years of work by some of the most innovative software and hardware developers in the semiconductor industry," said Chet Brown, president and CEO of IntellaSys. "Thanks to the algorithmic-configurable architecture embodied in our SEA Platform, our initial SEAForth family promises to enable a host of embedded wireless and portable applications." He noted that the company is currently in discussions with OEMs to become beta-site customers for its SEAForth-24 solution for handling distributed digital media processing in home theater environments.

SEAForth-24 Chip Profile

Combining a 6x4 array of 18-bit processors with a powerful set of I/O functions, the SEAForth-24 chip deploys an innovative dual-stack architecture that is both asynchronous and scalable. Capable of driving an antenna directly, the SEAForth-24 wireless solution eliminates the need for any external data converters. The numerous on-chip benefits include:

- RAM and ROM on each core (512 words each) to break the memory bottleneck
- Flash memory interface to ripple-load application code into cores at boot
- Static/dynamic RAM interface to facilitate common data memory access
- Real-time clock support in each core
- 18-bit A/D and 9-bit D/A to eliminate need for external data conversion
- Eleven Serial (SPI) ports, which can double as I2C, I2S, and USB ports
- 32 Parallel I/O lines with handshaking for versatile "bit banging"
- Scalable connectivity among multiple SEAForth-24 chips via high-speed I/O ports

With 24 cores operating independently on chip, designers can dedicate groups of them to handle specific tasks. For example, some could be assigned compute-intensive audio processing while others handle wireless/USB interfaces and drive external memory. Each core runs at the full native speed of the silicon instead of being throttled down to a slower external system clock frequency. At the same time, processors share the computing load by talking to each other to pass data, status signals, and even code blocks.

Each core automatically communicates with its nearest neighbors through dedicated registers. A core waiting for data from a neighbor goes to sleep to conserve power. Likewise, a core sending data to a neighbor not ready to receive also goes to sleep until that neighbor is ready. Even external signals on I/O pins wake up sleeping cores. By combining the automatic sleep mode with an asynchronous system architecture that eliminates an inefficient central clock, the SEAForth-24 chip operates at very low power.

VentureForth(TM) Programming Language

VentureForth(TM) programming language is the native machine code for the SEA Platform chips. As a RISC version of the well established Forth software language created by IntellaSys CTO Chuck Moore more than three decades ago, VentureForth provides 32 powerful instructions including full 18 x 18 bit hardware-based multiplies with 36-bit results. This simple but elegant version of Forth features fast hardware-based multiply/accumulates and micro FOR/NEXT loops for reading, sending blocks of data. Other features that relate to the way VentureForth runs on SEAForth chips include:

- Forthlet(TM) Code objects that can be stored in one core but executed on others
- Automatic "sleep mode" to save processor power while waiting to send/receive

-- RAM capacity for 2048 instructions; packing four instructions per 18-bit word

-- BIOS-facilitated message routing to assure efficient event coordination

VentureForth programming frees designers from laboring over thousands of lines of assembly code. Moreover, it creates extremely compact code that is quick to write and debug. User code is stored in each core processor's RAM. At boot time, code is loaded into the chip and ripple-loaded into the appropriate core processor's RAM. It is VentureForth that enables the SEA Platform to be easily scalable. This permits the deployment of a sea of processors ranging from dozens to hundreds of cores all communicating efficiently and effectively with one another -- whether cores reside on a single chip or multiple chips.

Development Tools & Forthlet(TM) Code Library

Central to the IntellaSys development platform is the T18 compiler and simulator to facilitate the design of multicore solutions that fully leverage the performance-per-watt benefits of its SEA Platform. Debugging is accomplished by using the simulator to watch each core execute code, set breakpoints, and interact with neighboring cores. The T18 development tools run on Windows, Macintosh, and Linux based platforms. In addition, evaluation boards featuring four of the SEAForth-24 chips plus a variety of compatible peripherals are being offered.

Extending the power of VentureForth is the Forthlet Code Library. Unlike conventional code libraries that require linking the entire library into the applications program if just one routine is used, the Forthlet Library links only the routines used. In this system, there is no penalty for building a large, comprehensive library. Routines in the Forthlet Code Library take the form of Forthlet code objects that can be moved around the chip from core to core to do special processing. Forthlets are the basic building blocks of code on the SEA Platform. They are used in the ROM BIOS in each core, and in the library of pre-coded functions. Even the user written program takes the form of a large Forthlet code object that calls the others. To make the user's programming task easier, IntellaSys currently offers designers a library of approximately 100 Forthlet code objects.

Distributed Digital Media Demonstration

To provide an early demonstration of the SEA Platform, IntellaSys has configured its initial SEAForth-24 chip to enable wireless operation of all speakers in a home theater application. Sophisticated and complete wireless control is achieved by installing a SEAForth-24 chip in each powered speaker and another in the receiver/amplifier to eliminate cumbersome speaker wires. As each speaker communicates with the receiver, it calibrates itself automatically to optimize audio performance in virtually any room environment. Each speaker knows exactly where it is in the room relative to others, and has intelligence to pick from the audio data stream its channel to reproduce in conjunction with the other speakers the highest quality audio. To further heighten the home theater experience, the audio "sweet spot" can be quickly moved to any point in the room with a simple click on the remote control.

Price, Packaging, Delivery

Assembled and tested in a 240-pin Ball Grid Array (BGA) package, the first SEAForth-24 chip solution will begin shipping in Q4 of this year. Priced at \$19.95 each in 1000-unit quantities, discounts will be offered on higher unit-volume orders. To expedite product development, an evaluation board featuring four of the SEAForth-24 chips plus a variety of compatible peripherals is being offered.

Industry Analyst Perspectives

"The real beauty of the IntellaSys SEA Platform is its asynchronous system architecture combined with a clever RISC adaptation of the Forth software language, developed by IntellaSys CTO Chuck Moore some 30 years ago," said Nick Tredennick, industry analyst and editor of the Gilder Technology Report. "While Forth software has successfully served a number of demanding applications over the years, including NASA's Cassini space probe, IntellaSys is well positioned to enable its broader use in embedded applications with its RISC version supported by a library of ready-to-use algorithms and object codes."

According to Tony Massimini, industry analyst and chief of technology for Semico Research, the low-cost of building microprocessors today has paved the way for integrating many of them on a single chip, operating them in massively parallel ways, and controlling them to conserve power and maximize speed. "IntellaSys has clearly pursued an exciting multicore path with its proprietary scalable platform. The company's innovative sea-of-processors deployment promises to deliver very attractive performance-per-watt price points for embedded applications."

About IntellaSys Corporation

IntellaSys Corporation is a TPL Group Enterprise focused on developing distributed digital media semiconductor solutions including multicore processors, Flash media storage products and content secure connectivity devices. With headquarters in Cupertino, California, IntellaSys operates eight design centers, four of which are in California as well as four others based in Tempe, Arizona; Castle Rock, Colorado; Cincinnati, Ohio; and Vienna, Austria. The TPL Group, founded in 1988, specializes in the development, commercialization and management of IP assets. For more information, visit www.intellasys.net.

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