

EE Times: Latest News  
Leakage mop-up begins

Anthony Cataldo

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By now, everyone knows about the serious problems that the chip industry is having with power dissipation at the leading edge of process technology. It seems that the aggressive scaling-down of voltage over the years has created a monster called leakage current, making Moore's Law a mere suggestion for many chip makers.

I've heard my share of Chicken Little predictions of events that were supposed to befall the chip industry, but I don't recall ever seeing the kind of unanimity of opinion that I have on this issue.

When Apple chose to switch from IBM to Intel processors, the decision was attributed in part to Apple's lack of confidence in the PowerPC's ability to hit performance targets within a given power envelope. Arthur Swift, president and CEO of processor maker Transmeta, said at a recent Semico Research conference that he has seen desktop systems canceled because of concerns over power dissipation.

Whether this means Moore's Law is dead is an interesting topic for debate, but not very useful. What's more important is to find ways to deal with the problem now.

Fortunately, there is some hope in the short term, according to companies that attended the Semico conference. A summary of their solutions follows:

Cadence, ARM and TSMC have collaborated on a low-power design that's supposed to reduce active and standby power in chips by 40 percent on average for 90-nanometer products. What's important here is that they've figured out a way to do it using a standard timing-closure flow and a middle-of-the-road process technology, said Mike McAweeney, vice president of industry alliances at Cadence Design Systems. Choosing the right mix of transistor thresholds, for example, now can be done automatically.

Japanese electronics giants Fujitsu, NEC and Sony are backing Transmeta's LongRun2 processor design. The key feature in LongRun2 is its ability to do threshold voltage control in standard CMOS. And if any of those companies wants to shift to a process, say, with high-k dielectrics, there's nothing stopping them.

NEC plans to use the design in everything from "cell phones to servers" at the 90-nm generation and beyond, Swift said.

National Semiconductor has come up with a voltage-monitoring device that can be implanted in a system-on-chip. Called PowerWise, the circuit monitors voltage in real-time and compares it with an estimate of what it should be so that the SoC can make the right adjustments. In this case, National has left it up to an ARM processor to make that decision. The companies have made a 0.18-micron test chip that has a power saving of 40 percent, said Dennis Monticelli, a Fellow at National Semiconductor.

What all these projects have in common is that each involves more than one player. Don't be surprised if more companies decide to share the burden. The industry needs as many engineers as it can muster to plug the leaks on this ship — at least until the guys in the lab build us a new one.

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