



Macros speed SoC static RAM integration

1T-SRAM Classic Memory Macros are a family of preconfigured high-density high-speed low-power memory macros using silicon-proven 0.13-micron cores.

<http://www.electronicstalk.com/news/mos/mos139.html>

News from: MoSys

Edited by: Electronicstalk Editorial Team on 16 June 2005

Available now from MoSys, 1T-SRAM Classic Memory Macros are a family of preconfigured high-density high-speed low-power memory macros using silicon-proven 0.13-micron cores.

By offering this set of macros in addition to its custom-designed embedded memory products, MoSys' customers now have the advantage of off-the-shelf, silicon-proven 1T-SRAM memory for rapid integration of high-density embedded memory into their SoC designs.

MoSys' Classic Macros are available in both high-speed and low-power configurations, targeted at applications including performance computing, high-throughput data networking, portable mass storage as well as high volume consumer entertainment and wireless personal communications.

High-speed Classic macros are available in 1Mbit configurations with 32, 64 or 128bit bus widths.

Speeds of up to 266MHz are supported.

The low-power Classic macros are available in 1, 2 or 4 Mbit configurations, all with 32bit bus widths.

The low-power offerings can operate at frequencies up to 133MHz and feature standby power of less than 80uA/Mbit.

All Classic macros employ MoSys' patented TEC technology resulting in higher yields, greater reliability and lower soft-error rates.

'Since its introduction, MoSys' 1T-SRAM technology has enabled designers to achieve significant performance advantages and cost savings', said Karen Lamar, Vice President of Sales and Marketing at MoSys.

'By taking advantage of MoSys' preconfigured Classic macro offerings, our customers now enjoy shorter design cycles and reduced development costs, while still retaining all of the performance benefits they have come to expect when using MoSys' technology'.

MoSys' Classic macros are licensed on single project use basis, and allow customers to use multiple instances in their designs to achieve larger on-chip memory sizes.

Classic macros are targeted for use with multiple foundries including Chartered, SMIC and TSMC, initially on the 0.13-micron process node.

Classic macro deliverables include datasheets, simulation and timing models, layout phantoms, GDSII databases and test documentation.

'With the new Classic macros line, MoSys is offering its customers immediate access to the best combination of high-density, configurable bandwidth and low power in an embedded SRAM memory solution'.

'Through use of its proprietary 1T-Q (single transistor, quad density) bit cell instantiated in Classic preconfigured macros, MoSys delivers truly compelling embedded SRAM memory solutions for immediate use as a drop-in replacement for larger, less-power optimised embedded SRAMs'.

'With Classic macros onboard their consumer and communications SoCs, MoSys' customers greatly accelerate their time to market while saving engineering development costs, particularly for SoC designs with increasingly aggressive market windows', said Rich Wawrzyniak, Senior ASICs and SoC Analyst with Semico Research.

'MoSys' Classic macros family greatly benefits fabless companies that do not have the capital resources or longer SoC design windows required to invest in a fully customisable 1T-SRAM solution'.

'Classic macros enable MoSys' customers to get the best bang for their buck by getting to market faster with optimal performance and significant cost savings'.

For customers with embedded memory requirements outside the scope of the Classic macros, including projects in advanced deep submicron processes such as 90nm, MoSys continues to provide its customised embedded 1T-SRAM memory macros.

MoSys 0.13-micron 1T-SRAM Classic macros are available now with pricing on request.

Silicon characterisation reports will be available by September 2005.