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## **MoSys Delivers 0.13 Micron 1T-SRAM Memory Compiler; Web-based Tool Compatible with TSMC, Chartered, SMIC and UMC Processes**

SUNNYVALE, Calif.--(BUSINESS WIRE)--June 13, 2005--MoSys, Inc. (NASDAQ: MOSY), the industry's leading provider of high-density system-on-chip (SoC) embedded memory solutions announced today the availability of its 1T-SRAM(R) memory compiler for standard 0.13-micron CMOS logic processes. The compiler targets processes from TSMC, Chartered, SMIC and UMC. The MoSys memory compiler is a web-accessible tool that automatically generates a wide variety of design scenarios for MoSys' 1T-SRAM memory, thereby enabling SoC designers to efficiently evaluate different memory configurations for their designs.

Available in July through the MoSys web site (<http://www.mosys.com>), the 0.13-micron compiler gives SoC design engineers complete control when assessing various options and benefits of implementing 1T-SRAM memory technology in their SoC designs. The compiler provides front-end design information, such as datasheets, simulation models and timing models for synthesis. It also allows SoC designers to include specific 1T-SRAM macro instances in their designs by generating place and route views and specifications for memory sizes, configurations, power, speed and temperature ranges. With this information on hand, all of the views required for simulation, synthesis, floor-planning and place and route of an SoC design are generated, allowing design engineers to quickly explore numerous "what if" scenarios. Upon customer licensing of the specified 1T-SRAM macro design, MoSys delivers the final GDSII database for customer tape out.

The MoSys 1T-SRAM compiler is targeted for both high speed and low power designs. When high speed options are specified, the compiler can produce macros capable of running up to 266 MHz with bus widths from 32 bits up to 256 bits wide. High speed macro sizes range from 1/2 Megabit to 4 Megabits. The low power options generate macros capable of achieving standby power of less than 80 micro Amps per Megabit, with clock frequencies up to 133 MHz and bus widths of 32 bits or 64 bits wide. Low power macro sizes range from 1/2 Megabit to 4 Megabits.

"We are delighted to enable and accelerate our customers' embedded memory SoC designs on aggressive process geometries," stated Karen Lamar, vice president of sales and marketing for MoSys. "MoSys' new 1T-SRAM compiler is an effective tool to help SoC designers ensure that they are generating the most optimized designs and making the best embedded memory technology selections for their product mix. We strive to make the process of integrating MoSys' technology into new SoCs as efficient as possible."

With the introduction of the 0.13-micron 1T-SRAM compiler, MoSys now offers customers a wide choice of options in design methodologies that include compiled, full custom and CLASSIC pre-configured memory macros. The MoSys 0.13 micron 1T-SRAM Compiler front-views generator is available now. The Compiler back-end optimizer is scheduled for release in the fourth quarter of 2005.

"The availability of MoSys' 1T-SRAM compilers, which are parametrically coupled with the CLASSIC macros product family, is an invaluable tool for MoSys' customers. The SoC design process is greatly facilitated by use of 1T-SRAM compilers, which allow for specification optimization, resulting in a quick turn drop-in embedded SRAM memory solution. It's a big cost and time savings for any semiconductor designer," said Rich Wawrzyniak, senior ASICs & SoC analyst with Semico Research.

## ABOUT MOSYS

Founded in 1991, MoSys (NASDAQ: MOSY), develops, licenses and markets innovative memory technologies for semiconductors. MoSys' patented 1T-SRAM technologies offer a combination of high density, low power consumption, high speed and low cost unmatched by other available memory technologies. The single transistor bit cell used in 1T-SRAM memory results in the technology achieving much higher density than traditional four or six transistor SRAMs while using the same standard logic manufacturing processes. 1T-SRAM technologies also offer the familiar, refresh-free interface and high performance for random address access cycles associated with traditional SRAMs. In addition, these technologies can reduce operating power consumption by a factor of four compared with traditional SRAM technology, contributing to making them ideal for embedding large memories in System on Chip (SoC) designs. MoSys' licensees have shipped more than 80 million chips incorporating 1T-SRAM embedded memory technologies, demonstrating excellent manufacturability in a wide range of silicon processes and applications. MoSys is headquartered at 1020 Stewart Drive, Sunnyvale, California 94085. More information is available on MoSys' website at <http://www.mosys.com>.

## FORWARD LOOKING STATEMENTS

This press release may contain forward-looking statements about the Company including, without limitation, benefits and performance expected from use of the Company's 1T-SRAM technology.

Forward-looking statements are based on certain assumptions and expectations of future events that are subject to risks and uncertainties. Actual results and trends may differ materially from historical results or those projected in any such forward-looking statements depending on a variety of factors. These factors include but are not limited to, customer acceptance of our 1T-SRAM technologies, the timing and nature of customer requests for our services under existing license agreements, the timing of customer acceptance of our work under such agreements, the level of commercial success of licensees' products such as cell phone hand sets, ease of manufacturing and yields of devices incorporating our 1T-SRAM, our ability to enhance the 1T-SRAM technology or develop new technologies, the level of intellectual property protection provided by our patents, the vigor and growth of markets served by our licensees and customers and operations of the Company and other risks identified in the Company's most recent annual report on Form 10-K filed with the Securities and Exchange Commission, as well as other reports that MoSys files from time to time with the Securities and Exchange Commission. MoSys undertakes no obligation to update publicly any forward-looking statement for any reason, except as required by law, even as new information becomes available or other events occur in the future.

1T-SRAM(R) is a MoSys trademark registered in the U.S. Patent and Trademark Office. All other trade, product, or service names referenced in this release may be trademarks or registered trademarks of their respective holders.

### Contacts

MoSys, Sunnyvale  
Walter Croce, 408-731-1820  
[wcroce@mosys.com](mailto:wcroce@mosys.com)  
or  
Shelton PR  
Katie Olivier, 972-239-5119 x128  
[kolivier@sheltongroup.com](mailto:kolivier@sheltongroup.com)

### At A Glance MoSys, Inc.

**Headquarters:** Sunnyvale, California  
**Website:** <http://www.mosys.com>  
**CEO:** Fu-Chieh Hsu  
**Employees:** 95  
**Ticker:** [MOSY \(NASDAQ\)](#)  
**Revenues:** \$27.8 Million (2002)  
**Net Income:** \$12.4 Million (2002)

*Source: via Business Wire  
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