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Power issues heat up chip forum

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(06/10/2005 12:22 PM EDT)

URL: <http://www.eetimes.com/showArticle.jhtml?articleID=164302132>

SAN JOSE, Calif. — A difference of opinion about power management strategy generated some heat, if not sparks, at the Semico Impact Conference on Intellectual Property here.

John Bourgoïn, CEO and president of MIPS Technologies, keynoted the one-day event with a talk about processor speed, memory bandwidth and the virtues of hardware-assisted multithreading.

Bourgoïn quoted from, "Computer Architecture: A Quantitative Approach." In that 1990 classic, RISC gurus John Hennessy and David Patterson first pointed out that — contrary to assumptions at the heart of the RISC concept — CPU execution speeds were rapidly pulling away from memory cycle times.

Bourgoïn argued that this gap has expanded to an oceanic 5,000:1 ratio between the time it takes memory to find an instruction and the time the CPU spends executing it. "The result is that a GHz-class CPU can spend half its time idle, wasting power," he observed.

Bourgoïn's answer is hardware multithreading. By giving the CPU the ability to switch cycle-by-cycle among multiple, ready threads, each with its own hardware context, Bourgoïn said every CPU cycle could execute useful work. How close to the ideal, he admitted, involved "a lot of magic in the policy manager and scheduler" that select the next thread for execution.

While no panelist disputed that multithreading could increase CPU cycle utilization, some disputed Bourgoïn's assertion that this was the best way to save energy in SoCs. Carl Schlachte, CEO of ARC International, argued that the best approach to energy savings wasn't hardware multithreading, which ARC doesn't currently support, but rather configuring inherently efficient CPU cores with the optimum execution units, datapath width and speed.

By omitting unnecessary hardware, and by minimizing instruction fetches with customized instructions, Schlachte suggested, power would be saved. "I don't see multithreading as a coming thing now," Schlachte said.

Mark Templeton, president of ARM USA, countered with a pitch for his company's current differential strength, hardware-based voltage and frequency scaling scheme. Templeton said the most energy efficient architecture for a thread-rich environment was not necessarily a single CPU — multithreaded, configured or not.

Instead, he showed data on a shared-memory multiprocessor cluster in which several identical ARM CPU cores, each with dynamic voltage and frequency scaling, were employed. Initially each core was powered down altogether, eliminating even leakage current. As the thread load increased, cores were powered up only to the voltage necessary to deliver the required performance for threads running on them. Thus, until full system throughput was required, most or all of the CPUs were running at reduced voltage, giving V² energy savings on each CPU cycle.

Grant Pierce, CEO of Sonics, added that most SoCs were in fact heterogeneous multiprocessors, with critical tasks loaded onto dedicated accelerators that could be optimized for both speed and energy.

Craig Lytle, vice president of systems engineering at Altera Corp, said the company has so far licensed 14,000 development kits for its NIOS-II CPU core. Lytle said Altera's sees great variation in architectural approaches. But he suggested that research design teams are using combinations of symmetric multiprocessing, implementation of specialized instructions and hardware accelerators — all readily implemented in FPGAs with the NIOS architecture.

"In one case, we saw a design team replace a board-level engine with 16 DSP chips with a single FPGA implementing four NIOS-II CPU cores, to each of which they had added eight additional instructions," Lytle reported.

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