

Memory IP Ready for 65nm

By Ed Sperling -- 7/21/2005

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Virage Logic today introduced its embedded memory design for 65 nanometers, a first step in gearing up the industry for the next major process node.

The move was considered essential for most developers of systems on a chip, as most of them have decided it isn't worth the time to develop their own embedded memory. Virage is the market leader in embedded memory intellectual property.

"Companies have to start development at least one year ahead and they have to have all the building blocks in place," said Rich Wawrzyniak, senior analyst at Semico Research. "It's essential that IP blocks at 65 are being announced, even if they are not starting production for two years."

So far, the number of companies that actually have started work on 65 nanometers is limited to the largest IDMs such as Intel, Texas Instruments, and two consortiums, one led by IBM that includes Infineon, AMD, Sony, Toshiba, Samsung and Chartered Semiconductor and another led by Philips that includes STMicroelectronics, TSMC and Freescale.

"There are pilot programs or designs that need to be implemented at 65 nanometers," said Wawrzyniak. "If they don't have the blocks ready, they can't do it at all."

Jim Ensell, VP of marketing at Virage, said there currently aren't a lot of customers adopting 65 nanometers, although he believes the platform will take off. Freescale has announced plans to adopt Virage's memory design, and UMC is working with Virage to determine how to best build it.

What happens after 65 nanometers remains a mystery, however. So far, Virage -- which needs to be well ahead of the market -- hasn't seriously begun looking at 45 nanometers or beyond. "The real issue there is who can justify the cost," said Ensell.

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