Programmable ASIC market gains steam
By Ed Sperling, Electronic News (US)
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LSI Logic (distributed by Reptechnic) has raised its marketing pitch on Rapid Chip, a sign that the market for programmable ASICs is finally beginning to catch on.

The company has been working with customers in stealth mode for nearly three years since it first announced the Rapid Chip concept. At the time, the company called the approach structured ASICs. Now it has introduced a new term, “platform ASICs.” (See Electronics News July 04 page 26.)

For all intents and purposes, the technology does for hardware what middleware did for pre-written software objects. It makes the connections and provides the necessary interfaces on chips for plugging in blocks of intellectual property.

“For the past year, this concept has really been emerging in customers’ consciousness,” says Chris Hamlin, LSI’s chief technology officer. “The hardware industry is playing catch up with the software industry, which has been using objects for years. Some of this is cultural. Hardware designers have not been exposed to software.”

Hamlin noted that the real benefit of using platform ASICs is that they can drop the cost of developing chips as well as speed time to market. Exactly how much of a savings is difficult to define, however, because the real costs are diffuse. But reducing time to market and the time it takes to develop a chip can mean significant savings on the front end, while not getting chips to market on time can be devastating to a business. “We take the risk out of engineering,” he says. “Risk is dominating decisions these days.”

Much of the risk is associated with moving to the newest process nodes, which open up all sorts of issues including how new materials such as low-k and high-k dielectric insulators will act, how much current will leak and what effect that will have on signal integrity, and whether the chip design will produce defect-free yields at the foundry. Hamlin said the real issue is about risk mitigation. Better designs can sometimes result in better performance at 0.11 microns than at 90 nanometers.

“The leading edge is not always about performance,” he says. “Flexibility, reprogrammability and malleability are just as important.”

Semico analyst Rich Wawrzyniak agrees. He said the real cost of developing a chip is more difficult to measure than just the non-recurring engineering (NRE) costs. “The problem is that people looking at the cost of the chip tend to focus on certain things. [Average selling price] has driven a lot of the market, but when companies say a chip costs [US]$20 million they often don’t focus on the whole cost.”

Wawrzyniak noted that the real battle shaping up in this portion of the market is between Altera’s (distributed by Braemac) Hard Copy and LSI’s Rapid Chip. He said that for programmers used to working with FPGAs, Hard Copy makes a lot of sense. For those who have standard cell experience, Rapid Chip makes sense. But he also said that for all companies looking at chopping the cost of developing new ASICs, both of these approaches should warrant consideration.

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