

Structured ASIC Market to Grow to \$1.4B, Semico Says

Online staff -- 7/16/2004

Electronic News

<http://www.reed-electronics.com/electronicnews/index.asp?layout=articlePrint&articleID=CA436979>

Shrinking market windows, lengthening design cycle times, higher design costs and shortened product life cycles are fueling the structured ASIC market and will provide it with the momentum to expand into the future, from \$164.1 million last year to \$1.4 billion in 2008, a CAGR of 54.4 percent, according to Semico Research Corp.

This market segment has breathed new life into an ailing ASIC market by allowing a large group of former users of ASIC products to return with a major source of structured ASIC revenue coming from previous ASIC users that were contemplating the use of standard products for their next design, the Phoenix, Ariz., market research firm said.

Many former ASIC users had been unable to continue using ASICs due to factors such as the rise in development costs for standard cell and SOC designs, a lack of competitive offerings from the gate array industry in terms of performance and gate count, a lack of design resources or expertise to undertake an extensive design using standard cell or SOC approaches and the high cost of FPGA silicon which limits the volume at which FPGAs can participate in many applications.

Semico forecasts unit volumes for the structured ASIC market to grow from 11.7 million last year to 81.9 million units by 2008, a CAGR of 47.5 percent.

Average selling prices (ASP) for structured ASICs is forecast to be relatively flat over the forecast period reaching \$17.61 in 2008, up from \$14.03 last year, representing a CAGR of 4.7 percent. One reason for the high ASP is the relative die area inefficiency of structured ASICs relative to other ASIC types due to the large number of transistors needed per gate in structured ASICs compared to standard cell designs. This trade-off is acceptable considering the short time to market for structured ASIC and the low entry cost for a structured ASIC design, Semico said.

Although the cost of structured ASIC silicon is higher than that for standard cell, gate array and SOC silicon, the total 'cost to create' a structured ASIC is still lower than for the other alternatives. Further, the revenue forecast for structured ASICs could prove to be conservative depending on how many vendors move their product portfolios to production using 90nm geometries as smaller geometries allow for much less expensive silicon over time.

This perspective translates into a number of trends influencing ASICs today including the evolution of structured ASICs, the role of structured ASICs in closing the design productivity gap, and the impact of structured ASICs on future process geometries as mask set costs continue to increase, that Semico addresses in a recent report.

© 2004, Reed Business Information, a division of Reed Elsevier Inc. All Rights Reserved.