

IDT - Industry's first off-the-shelf statistics engine

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Enabling system designers to develop new value-added services and functions, IDT (Integrated Device Technology) has announced the industry's first off-the-shelf statistics engine. Targeting edge router, broadband access equipment and multi-service provisioning platforms, the IDT statistics engine features a network processor forum (NPF) look aside (LA-1) interface and offloads processor elements such as NPUs, FPGAs and ASICs of the critical function of statistics tracking.

With the new single-chip device, designers can focus on other compute-intensive functions related to meeting the requirements of IP-based services, including the transition from IPv4 to IPv6 and the deployment of content-rich services that tie revenue to comprehensive and accurate tracking of bandwidth consumption, such as streaming media and online gaming, says the company.

"The introduction of the statistics engine is yet another step in our ongoing effort to couple systems-level application understanding with our various technologies to deliver value-added solutions that improve upon performance and cost effectiveness," said Michael Miller, IDT chief technology officer and vice president of the Systems Technology Group.

"Customers looking to design a 10G (OC-192) edge/access/metro router, coupled with a current-generation packet processor, will experience difficulty achieving line rates when supporting thousands of customer flows. This equipment requires differentiated services, and maintaining quality of service and service-level agreements at line rates with a single processor design is nearly impossible. By preventing the processor element from stalling on the restrictive external bus transactions, the IDT statistics engine will play a critical role in helping customers overcome system-performance challenges."

Bob Merritt, vice president at Semico Research Corp, said: "As the industry continues the development of advanced services via packet-switched networks, the task of statistics monitoring has significantly grown in importance, with service providers needing to provide guaranteed bandwidth for applications such as VoIP and other content-rich data. The IDT statistics engine addresses an important need in the market and offers several advantages over previous statistics-gathering solutions, enabling service providers to offer a richer set of options to their customers."

Edge and access equipment must maintain counters for thousands of customer flows, which is beyond the on-chip storage of today's NPUs and ASICs, thus requiring off-chip storage. With today's internal processing elements operating in excess of 1GHz, stalling on multiple external multi-clock read cycles per packet for flow statistics is very costly. Stalls often require processor threads to context switch, further adding to complexity and overhead, which can exceed design budgets, says the company.

The new statistics engine uses an integrated 64-bit arithmetic logic unit (ALU) designed to offload data-path processor cycles, typically resulting in a 90 percent improvement in network processor cycles required for statistics computation. This allows designers to increase the line rate of packet processing and execute deeper packet inspection to support new IP-based services.

The ALU coupled with the enhanced multi-port memory cell architecture enables the statistics engine to update multiple counters with an innovative, patent-pending 'fire-and-forget' operation. Fire and forget is an atomic operation that replaces the conventional read-modify-write sequence, and allows the processor element to access and update as many as four counters on every clock cycle. The

benefits associated with the fire-and-forget function include up to 87 percent improvement in QDR-II bandwidth. This feature will be especially useful to software designers who up until now, have relied on cycle-consuming read-modify-write routines in their code.

The enhanced multi-port memory cell architecture of the IDT statistics engine also ensures coherency for low-latency statistics operations that require multiple statistics updates every five nanoseconds, a capacity that becomes important at 10G and above line rates. The configurable 64/32-bit ALU is also useful for systems that need to upgrade their legacy 32-bit operations to 64-bit operations without incurring performance penalties. These configurable options, offering customers either 512K 32-bit counters or 256K 64-bit counters, allow the on-chip memory resources to be efficiently partitioned to match the system applications, such as traffic engineering and billing.

Because the statistics engine is a single-chip, off-the-shelf solution, board designers realize benefits such as lower system costs, reduced board complexity and improved time to market. In addition, the device's ability to 'clamshell' to x18 burst-of-two QDR-II SRAM lends itself to ease of board design while addressing the emerging trend towards standardization in network systems. The IDT statistics engine is available in a 576-ball, RoHS-compliant flip-chip package, says the company.