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Arrays narrow platform ASIC, FPGA gap

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Narrowing the performance and density gap between FPGAs and structured or platform ASICs, a novel configurable array architecture unveiled by startup CSwitch Corp. promises to deliver levels of flexibility not previously available in programmable products.

The flexibility is achieved by combining elements that can move, edit and store data packets at performance levels comparable to full-custom processor designs. CSwitch claims the architecture, which achieves data bandwidths of 100Gbps, can be applied across a wide range of high-performance networking, storage, telecom and wireless-base-station applications, while providing the ability to modify or upgrade features via software-configuration downloads.

To achieve high throughput, the basic architecture of the configurable switch combines an array of custom-compute and -control elements and a high-bandwidth programmable interconnect structure that internally transfers 20bit-wide data across the chip at 2GHz.

"That combination lets the configurable switch array deliver the flexibility of an [FPGA](#) and the high throughput of a custom processor," said Doug Laird, president and CEO of the company. "The challenge is to keep the chip flexible so that it can be used in a wide range of applications. If the functions are too application-specific, the market niche will be too small to support the development activities."

"Such configurable architectures could fill a gap between high-end FPGAs and structured or platform [ASIC](#) solutions," said Bryan Lewis, research VP at the Gartner Group. CSwitch is targeting the structured-ASIC market, which in 2010, is expected to claim about \$1.3 billion, or roughly 3.5 percent of the \$31.4 billion total ASIC market, according to Gartner.

Although that predicted figure represents growth from the estimated \$400 million structured-ASIC segment today, it's also lower in percentage terms than the 5 percent ASIC market share that structured ASICs are predicted to claim in 2008, said Lewis. The decline in market share between 2008 and 2010, he said, "will be caused by the forthcoming generations of finer-geometry processes that will be used by high-performance FPGAs," along with the arrival of field-programmable alternatives such as the CSwitch offering and a field-programmable object array developed by MathStar Inc.

It is still unclear, however, whether the companies offering the new alternatives will be able to provide the library support, staying power and alliances to satisfy their potential customer base, said Lewis.

Traditional FPGAs are very generic, but some of the higher-end FPGAs, such as Xilinx Virtex 4 and the just-released Virtex 5 families, offer multiple subfamilies, each optimized for a different market segment. The optimizations are achieved by crafting different mixes of memory, logic, multiplier-accumulator (MAC) blocks and high-speed I/O (e.g. multigigabit Serdes and differential or single-ended buffers).

By contrast, structured ASICs, such as those offered by Altera, AMI Semiconductor, eASIC, Faraday, Fujitsu, NEC and others, use one or more customized metal layers to configure the logic. That limits their in-system flexibility compared with RAM-based field-programmable solutions. Most structured solutions also involve significant non-recurring engineering fees related to the custom metal interconnect layers, said Laird.

RAM-based FPGAs use multiple-input look-up tables (LUTs) as the programmable logic element, and all of the complex functions are built up using the LUTs and MAC blocks. Making FPGAs even more application-specific by integrating higher-level configurable functions can narrow the market opportunity, Lewis said. But the higher-level functions would allow such FPGAs to deliver better performance than generic FPGAs and comparable performance to that possible with a structured ASIC.

The general logic fabric of FPGAs implemented at the 90nm process node has an upper speed limit of about 500MHz when signals go across the chip. That will limit the more complex functions built up from the fabric to top operating speeds of a few hundred megahertz, according to Rich Wawrzyniak, senior analyst at Semico Research Corp. "By integrating application-specific functions into a configurable fabric, the programmable chips can deliver higher operating speeds, but the challenge of defining the larger application-specific functions puts more of a burden on the chip designer," he said.

In some cases, field-programmable function arrays like the CSwitch and MathStar architectures will go after the same markets as structured ASICs, Wawrzyniak said. In most cases, however, "the design decision will come down to price and performance trade-offs, and possibly even to the tool suite that the designer must use for configuration."

Tools in the works

Silicon won't be available until Q4, but designers at CSwitch have been working with Magma Design Automation Inc. to craft a suite of design tools that will allow designers to turn RTL designs into programming bit streams to configure the array. The tool suite will provide a unified flow, offering a complete logical-to-physical mapping of a design from RTL to all ASIC and FPGA platforms, including synthesis and placement, routing and optimization, and bit-stream generation to configure the array.

The tools will leverage a library of functions that CSwitch is developing, along with Magma's established logic design flow, said Sanjay Bali, product director of the design implementation business unit at Magma. The first library of functions will focus on network-related applications. Later libraries will support storage, telecom and wireless-base-station applications.

The custom-configurable elements on the chip include packet parser blocks that operate at 800MHz for header parsing and multiple configurable blocks that all can run at 1GHz. The latter include reconfigurable content-addressable memories (RCAMs); reconfigurable arithmetic units for packet editing; and dual- and single-port SRAM blocks. Also incorporated on the array are programmable-logic blocks that can operate at 500MHz.

FPGAs typically contain generic programmable-logic blocks, general-purpose blocks of SRAM and, in some cases, high-speed Serdes blocks. Laird said the CSwitch configurable array's dedicated blocks deliver higher performance than FPGA logic while offering similar flexibility levels.

Interconnecting all the on-chip functions is a novel data cross-connect bus structure that operates at 2GHz. Unlike the programmable interconnect wires used on FPGAs, the cross-connect structure uses 20bit-wide data paths, said Laird. "These wide buses transport the packets all around the chip, thanks to special crosspoint interchanges that allow the 'east-west' and 'north-

south' buses to transfer data at key intersections," he said, adding that the Magma design tools have been enhanced to recognize the special data cross-connect features and leverage them in the synthesis flow.

The array architecture's blocks of programmable logic are similar to the logic elements in FPGAs. Based on four-input LUTs clocking at up to 500MHz, the blocks handle basic control functions and provide the logic glue between the dedicated function blocks and various system interface functions.

The architecture's reconfigurable CAMs can be configured as ternary or binary CAMs or as RAMs or programmable logic arrays. Surrounding the configurable core are full-duplex Serdes blocks capable of 1-6.4Gbps data transfers; configurable MACs; high-speed memory controllers for external memory; and lots of configurable general-purpose I/O buffers.

Every interface on the chip is highly configurable. For instance, the Serdes ports can be configured for PCI Express, Xaui, Fibre Channel or GbE compatibility, while the MACs can be set up for 10/100/1000Mbps Ethernet, 1/2/4Gbps Fibre Channel or 10GbE operation. The multiple memory controllers can be set up for 36bit or 72bit interfaces, and they support DDR2, RLDRAM II or QDR II memory types.

For general-purpose interface support, the chip contains configurable I/O lines that handle data rates of 1.25Gbps in differential mode or 1.07Gbps in single-ended mode.

- [Dave Bursky](#)
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