

EE Times: Design News  
Startup looks to hit ground running with two-pronged model

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SAN FRANCISCO — A Santa Clara, Calif. startup has emerged to focus on designing ASICs and system-on-chips (SoC), implementing specialized techniques for RF CMOS, high-voltage, low-power mixed-signal and digital design.

The company, Key ASIC, has a two-pronged business model: to sell intellectual property (IP) and design-to-manufacturing (DFM) services, and to market its own communications and consumer electronics chips as a fabless ASIC company.

The company, founded in October 2005, already has a number of IP and services customers, according to Alan Aronoff, vice president of marketing and business development. In fact, Aronoff said, Key ASIC expects to turn a profit this year. Aronoff said the company expects that the majority of revenue in 2006 will be generated by IP and services, but also expects to generate revenue from chip sales toward the end of the year.

Key ASIC's primary technology offering is the KeySoC platform for ASIC/SoC DFM, targeted at reducing customer design time and enabling first time silicon success, the company said. The platform provides an ARM-based CPU platform with a high-performance CPU core and memory blocks for integration of domain specific IP blocks to design ASICs or SoCs quickly, according to the company.

The platform is specifically targeted for a variety of communications and consumer electronics applications, Key ASIC said. The platform also consists of a wide selection of silicon proven interfaces, the company said.

"We are seeing great demand for integration of multiple functions onto a single piece of silicon that has to fit into a very small form factor and this need is prompting companies to outsource the design and manufacturing of these targeted ASICs and SoCs to companies with extensive real-world expertise in consumer electronics and communications," said Kah Yee Eg, Key ASIC founder and CEO. "Key ASIC is the company that will be leading the charge."

Key ASIC said it has formed partnerships with top semiconductor foundries, strengthening its DFM service offering. DFM service engagements can begin at three different levels, Key ASIC said, ranging from high-level specification to GDS II, with Key ASIC delivering tested and packaged chips or tested wafers.

According to Key ASIC, it can, based on detailed customer ASIC specifications, design at RTL, going through RTL simulations, synthesis and gate level simulation. Upon successful completion of the gate level simulation, the company will perform physical implementation, parameter extraction and post layout timing analysis before producing a GDSII file, Key ASIC said. Customers can give Key ASIC a thoroughly verified netlist and the company will provide place-and-route services and extractions, the company said.

Through its KeyIP service, Key ASIC offers customers the ability to license IP from its pool of mixed-signal and digital IP, including interfaces, IP blocks, CPU and DSP cores, the company said.

"During a seemingly difficult time to start up an ASIC design company, especially with some industry discussion about the future of ASIC technology, Key ASIC is coming to market with a more complete solution than most advanced players," said Rich Wawrzyniak, senior analyst for ASICs and SoCs at market analyst Semico Research Corp. "The company's targeted offering is filling a necessary niche and has the potential to be very successful with its array of CE engineering talent, diverse locations and top-tier partners to support customers throughout the design-to-manufacture process."

In addition to Aronoff and Eg, both industry veterans and former Synopsys Inc. executives, Key ASIC is led by Jim Lang, vice president of North America sales (a former senior executive at Cirrus Logic, Adaptec and ARC) and Chan-Woo Nam, vice president of sales, Asia, a 25-year sales veteran of Synopsys and Cadence Design Systems Inc.

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