

Configurable platform caters to video

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After visiting about 60 companies during his first year as CEO of ARC International, Carl Schlachte was fascinated by the large number that had licensed ARC's configurable architecture and then spent time paring it to the bare necessities.

"Configurability for these companies was all about taking things away," he said. "Even when they added custom extensions and changed the instruction set, it was really with an eye toward removing things, like the need for extra clock speed or some of the on-chip memory."

Engineers were trying to create a device that was optimally suited for the application they had in mind. That jibed with the former chip designer's belief that there are no free transistors—not even in the 90nm era. And that thought is at the heart of ARC's new configurable video offering.

These days, Schlachte is busy rallying support for ARC Video, a 260,000-gate platform based on an ARC 700 family core that is coupled with the company's single-instruction, multiple-data (SIMD) accelerator and DMA engine. The SIMD accelerator was developed to exploit the data parallelism inherent in media applications, with a single instruction able to compute up to eight separate 16bit video pixels simultaneously through the use of a 128bit-wide datapath. Supported codecs include H.264, VC-1, MPEG-4 and MPEG-2, as well as numerous image files.

Market watcher Semico Inc. predicts that although 32bit configurable cores will still be dwarfed by fixed architectures in the next few years, the segment will enjoy a CAGR of 45 percent through 2010, when the units shipped are expected to top 900 million. "It will take a few years for us to see its impact," said Tony Massimini, chief of technology at Semico. "So the design work we are seeing in 2005 and 2006 will not really come to fruition until 2008 or 2009, when we'll start to see high growth."

That will draw others into the game. "Certainly, it would not be surprising to see the larger processor-core companies become interested in this market," said Jordan Selburn, an analyst at iSuppli Corp. "It's not a good idea to discount the size and market presence of ARM, and I'm sure Tensilica and ARC are both very aware of the possibility of competing with ARM. The existing configurable-processor vendors have some solid momentum going and I would expect they could weather the competition."

ARC hopes that its video offering is well-timed to coincide with the rising popularity of media-centric smart phones, PDAs and personal media players, as well as to nip into the more mature markets, such as digital still cameras.

ARC believes many designers are looking for the flexibility that configurable cores offer. That may hold especially true for designers at companies looking to stand out in the competitive and power-sensitive communications market, where most configurable cores will be used.

So like ARC's earlier platforms, the video subsystem can be altered to handle more than just decoding video at QCIF and QVGA or at standard-definition VGA and D1. Designers can use the ARChitect system-configuration tool to tinker with removing memory or with the memory-management unit, or to change register files and get rid of optional extensions. More important, it's possible to add custom extensions back into the architecture to perform such tasks as post-process scaling, noise reduction or color-space conversion.

While it's possible to use non-ARC host CPUs with the video subsystem, ARC is touting its 700 family of cores as suitable for the companion CPU. It's also focusing attention on the ability of the core to bounce from low-performance demands of simple system control up to increasingly complicated tasks of handling MP3 decode or standard-definition video resolutions that might require coprocessors or dedicated hardware blocks.

"What you're seeing as you move up is complex architectures with incompatible instruction sets—maybe you have one instruction set for the CPU, another one for the coprocessor, and you could probably cobble something together for your state machine and dedicated hardware blocks," said Dan Davis, ARC's product-marketing director. "It makes for a very difficult programming environment, and it's very difficult to migrate your code."

In the video subsystem, ARC highlights the efficiency of using a macro memory tied to the SIMD engine. For algorithms that process similar operations repetitively, that set of instructions can be sent through the code queue once and written into the macro memory. The SIMD engine can execute the operation from there, letting designers decouple the accelerator from the CPU, which can carry out parallel tasks.

ARC reckons its subsystem can decode any of the algorithms it provides at less than 44mW for D1 resolution. Because it's based on an ARC 700 core, the subsystem can run at up to 533MHz in a 0.13µm process and developers can use the same software development tools.

"You will always find lower-power solutions, but they are hardwired solutions that do MPEG-4 or H.264 only, and they are optimized. This is multistandard and programmable," Davis said.

Later this year, ARC will enhance its ARC Sound platform to offer high-speed audio encode and multistream decode. Coming next is video encode. A decode platform for HD video is planned for late 2007.

- Mike Clendenin
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