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EE Times: Semi News

TSMC sees low-power process as new technology driver

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(04/27/2005 4:13 PM EDT)

URL: <http://www.eetimes.com/showArticle.jhtml?articleID=161601168>

SAN JOSE, Calif. — Changing its strategy in midstream, Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC) this week made a major but overlooked announcement: The silicon foundry giant is moving from high-performance to low-power processes as its future technology driver. At the TSMC Technology Symposium here on Tuesday (April 27), the company dropped hints about a new and proprietary strained-silicon technology that is supposed to address troubling power issues in chip design.

TSMC (Hsinchu, Taiwan) also revealed its new 80-, 65- and 45-nm processes. The main emphasis at the event was the company's new and long-awaited 65-nm process, declaring that first wafers processed with the rules are expected in December.

The first offering from its 65-nm process is expected to be a low-power platform or technology, which represents a new strategy for the company, said Kenneth Kin, TSMC's senior vice president of worldwide sales and service.

In the past, TSMC moved in step with Moore's Law and emphasized its high-speed processes as its technology driver. "It's not that we're de-emphasizing speed," Kin said in an interview. "We're just shifting our priorities. We are going to use low power as a technology driver."

The move reflects the overall direction of the semiconductor industry, where power has become a stumbling block in chip design. For example, moving towards lower-power products, Advanced Micro Devices Inc. and Intel Corp. are separately scrambling to develop and ship dual-core processors for PCs.

TSMC is seeing a similar trend, especially in cellphone design. "The baseband developers are the first ones to move to the next technology node," Kin said. "We are responding to market needs."

This is not to say that TSMC will fall behind against its rivals in the foundry technology race, said F.C. Tseng, deputy chief executive for the foundry giant. In the 65-nm process-technology race in general, for example, the Taiwan company is only "a month or two" behind Intel and running neck-and-neck with leading integrated device manufacturers, Tseng told EE Times.

## Market worries

What really appears to worry Tseng is the slowdown in the IC industry, lack of killer applications and escalating design costs — all of which will affect the growing but mature foundry business.

During the 1980s, the overall semiconductor industry grew at an average rate of 15 percent a year, Tseng said. In comparison, the industry is projected to grow only 10 percent a year through 2010.

In total, the foundry business hit \$16.3 billion in sales in 2004, according to TSMC. In the pure-play arena, TSMC was the leader in terms of market share with 47 percent of the business in 2004, followed by UMC (23 percent market share), SMIC (6 percent), Chartered (4 percent) and others (17 percent).

In 2005, the foundry business is expected to slow down. Len Jelinek, principal analyst of market research firm iSuppli Corp. (El Segundo, Calif.), projects that the overall IC industry will grow faster than the pure-play foundry business in 2005, due in part to the current and ongoing down cycle. In 2005, iSuppli projects that the overall IC industry will grow 6 percent over 2004.

The slowdown is prompting TSMC to switch gears in its overall strategy. Last year, TSMC unveiled its so-called platform strategy. In this effort, TSMC had two platforms: advanced technologies and mainstream processes.

At this year's event, the company outlined a two-pronged approach: advanced technologies and derivatives or specialty processes. The change appears to indicate that TSMC is de-emphasizing its more mature and lower-margin "mainstream" technologies, leaving those processes on the table for the fledgling foundries in China and the rest of Asia.

"I am sure that TSMC is not going to abandon customers," said Joanne Itow, an analyst at Semico Research Corp. (Phoenix). "They appear to be focusing on the technologies with higher margins. That is their forte."

#### New strategy

Another change in strategy involves its emphasis on low-power processes. For years, when TSMC moved from one technology node to another, it would first debut its "high-speed" process.

Now, TSMC is shipping its 90-nm process technology. But bridging the gap between its 90- and 65-nm processes, the company is quietly ramping up an 80-nm technology.

On its logic roadmap, TSMC is working on various versions of its new 80-nm process, including three platforms: general purpose, low-power and high-speed technologies. The first offering to the market will be the high-speed process, which will move into "risk production" in the second half of this year, according to TSMC (see April 26 story).

But starting at 65-nm, the company will first offer its low-power process, followed by its separate general purpose and high-speed offerings. The 65-nm process itself is a nine-level metal technology equipped with copper interconnects and low-k dielectric materials, based on carbon-doped oxide. The gate materials will be based on a salicided-poly silicon dioxide, while the technology will also deploy nickel silicide as well.

The 65-nm technology will reportedly make use of a new and proprietary strained-silicon technology to boost transistor mobility, although the company did not discuss the process. TSMC's strained-silicon technology reportedly will also be used in future processes, including its yet-to-be-introduced 45-nm offering.

TSMC also presented a sneak preview of its 45-nm process technology, which is due out in the 2008 time frame. The foundry plans to deploy copper, ultra low-k dielectrics and immersion lithography at the 45-nm node, said TSMC's Shang-yi Chiang, senior vice president of R&D.

TSMC is exploring high-k dielectrics for gate stacks, of which it would like to use at the 45-nm node, according to analysts. But Chiang does not believe that high-k dielectrics would be ready for the 45-nm node, forcing the firm to extend traditional silicon dioxide materials and other technologies in the arena.

"My personal opinion is that (high-k) will not be ready," Chiang said in an interview. "The materials are very difficult."

In a keynote address, the TSMC technologist said the company is researching high-k, based on hafnium materials. But the company believes that it can gain more improvements in transistor mobility by using strained-silicon technology.

Chiang did not provide details about the technology, but noted the company plans to move towards a new low-k material at 2.4-to-2.5 for 45-nm, based on carbon-doped oxide technology.

TSMC's 45-nm process will move into "risk production" in 2008, he added.

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