

Process innovation drives design advancement

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The semiconductor industry continues to double transistor density almost as if to prove Moore's Law. The need to upgrade the underlying technology is driven by economic common sense. As demand peaks, you have to introduce new production technology that drives sales of production equipment that enables smaller, more powerful and cheaper ICs, which in turn result in better and cheaper end-user devices. The circle, virtuous or vicious as you like, progresses indefinitely.

It seems like only yesterday when we got all excited about the 90nm node. We were debating its commercial viability, fretting if production equipment would be ready in time for the next upswing in semiconductor demand and talking about Intel's experience with yields at 90nm. No one was discussing the 65nm process, let alone the 45nm and beyond.

Even as 90nm evolves toward maturity, research persists into the next generation of process technologies at facilities such as those of IMEC, a Belgium-based research center. In October 2004, IMEC and the Crolles2 Alliance—partnership of Philips, Freescale and STMicroelectronics—announced the development of an advanced RF CMOS process at 90nm. In the same breath, Philips announced the publication of papers on 65nm, 45nm and sub-45nm technologies.

The same month, IMEC claimed a breakthrough toward 45nm manufacturing with the integration of fully-silicided nickel silicide (NiSi) gates on top of high-k gate stacks. Intel Corp., which claims to have developed a high-k gate stack, plans 45nm chip production in 2007, 32nm in 2009 and 22nm in 2011, according to Tim Mohin, director of sustainable development, in a recent interview.

And just last month, Fujitsu disclosed its plans to use carbon nanotubes to replace some of the copper interconnects between circuit layers on an IC. The company sees carbon nanotubes as the answer to the problem of electromigration in copper at 45nm and below processes. Fujitsu's nanotubes are expected to measure 5nm to 10nm in diameter and have the ability to carry about 1,000 times the current density of copper. The company has reportedly experimented with 1,000 connections using the carbon nanotubes on test chips and is considering the use of nanotubes for some of its 45nm ICs made after 2010.

The ever-increasing pace of technological development, however, comes at an ever-increasing cost. The growth in R&D costs in the semiconductor industry has been surpassing its revenue by 4 percent each year, according to Hans Stork, chief technologist at Texas Instruments, at the Semico Summit last month. If the trend continues, it would restrict innovation at the semiconductor level.

Each significant development in the manufacturing process is accompanied by advancement in design automation technologies—up one level abstraction or a step sideways to better deal with issues at some stage, for instance, verification. As 90nm processes and below enable a level of integration that allows systems to be built onto chips, a design gap is looming that cannot be addressed just by going up one level of abstraction, but by taking a systems view of a chip. The days of IC and software designers working as separate teams are numbered. The return-on-investment in manufacturing R&D hinges on design advancement.

While we love talking about SoCs, are we really ready for this leap into the next generation of IC design? Are the tools we use able to support the system-level perspective we desire? Do the companies we work for have development strategies in place for 90nm and finer processes? These are some of the questions EE Times—Asia will ask you next month when we update our

understanding of your design successes and challenges with the annual "Design Trends & EDA Tools" survey. I look forward to your feedback.