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## Start-Ups Add Third Dimension to Chips

*Start-Ups Squeeze In More Features by Breaking From Two-Dimensional Designs*

By DON CI ARK

A perennial race to squeeze more features on flat pieces of silicon is taking a step into the third dimension.

Two Silicon Valley start-ups are breaking from conventional designs—which lay out components on chips in two-dimensional patterns—to develop products that are configured by customers after they are manufactured. Such programmable chips are a popular choice for some devices, such as computer-networking gear, but are considered too expensive for many high-volume applications.

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Gary Parker Photography

Tabula's chief executive, Dennis Segers, pictured next to images of the San Jose, Calif., start-up company's innovative chip designs.

Tier Logic Inc. and Tabula Inc. disclosed plans earlier this month to address that problem. They

say their technologies add functions to chips without expanding their surface area, which tends to add materials and processing steps that increase manufacturing costs.

Tier Logic, a closely held company in Santa Clara, Calif., says it plans to layer transistors and other components in a novel way. "They are stacked in multiple stories," said Paul Hollingworth, the company's vice president of sales and marketing.

The chips' basic functions are handled by a foundation layer of circuitry, created using standard production processes, the company says. On top of that, a special extra layer of memory circuitry stores programming instructions that customers choose for specific applications. Such memory cells, as they are called, tend to add to the size of two-dimensional programmable chips.

Tier Logic builds its cells using what the industry calls thin-film transistors, a technology that is more often used in computer displays than chips. Metal circuitry can be substituted for the memory layer, converting a programmable chip into a chip that is customized for specific applications.

Tabula, of nearby San Jose, Calif., views time as a third dimension. Instead of creating a new physical structure, the company says, it has devised a way to break up designs into eight sections called folds that are successively loaded into its chips, executed and replaced.



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Dennis Segers, Tabula's chief executive officer, says the reconfiguration happens so quickly that it appears like all eight sections are working simultaneously. "It looks to the world like it is an eight-layer array," he said.

The idea of breaking from two-dimensional designs isn't new. Researchers at companies such as [Intel Corp.](#) and [Advanced Micro Devices Inc.](#), for example, have developed prototype three-dimensional transistors as candidates to eventually be used in chips.

A Silicon Valley start-up called Matrix Semiconductor Inc., purchased in 2005 by [SanDisk Corp.](#) for about \$250 million, developed a three-dimensional technology for memory chips. But SanDisk says commercial products using the 3-D technology remain two or three years from the market.

There are plenty of reasons to ride existing technology. Companies keep finding ways to shrink transistors, boosting capabilities of chips while lowering the cost of each function they deliver.

The two big makers of programmable chips, [Altera Corp.](#) and [Xilinx Inc.](#), benefit from the miniaturization. While more advanced production processes make it more costly and complicated to design custom chips from scratch, reconfigurable chips become economical for more applications, executives of the two companies argue.

Still, high-end versions of such chips—known as FPGAs, for field programmable gate arrays—can be costly. Tabula's Mr. Segers says it is initially targeting FPGAs that cost \$1,000 or more; his company expects to handle comparable tasks with a chip dubbed Abax, which is priced at \$150 and is expected to be shipped in sample quantities in the third quarter.

Tier Logic hasn't disclosed pricing. But Mr. Hollingworth estimates its programmable chips—expected to ship in sample quantities in the second quarter—will be about half the price of a comparable FPGA.

The company's other versions emulate conventional products known as ASICs, for application specific integrated circuits. Mr. Hollingworth says adapting an FPGA version that a customer has programmed to an ASIC takes about four weeks, compared with 14 weeks using existing approaches; though comparable ASICs cost less to manufacture, low up-front design costs typically make Tier Logic's approach more affordable, he says.

Rich Wawrzyniak, an analyst at Semico Research Corp., calls the cost structure of both companies' technology "very attractive." He estimates that sales of all programmable chips in 2009 declined 12% to \$3.3 billion, but expects revenue to grow as much as 30% this year.

The sales potential has attracted many FPGA start-ups before, Mr. Wawrzyniak and other analysts are quick to point out. Most have faded before building significant businesses.

Krishna Rangasayee, Xilinx's vice president for corporate strategic planning, argues that it isn't enough to have a promising technology. A company must prove it can repeatedly meet customer needs over two or three product generations.

"It's a five- to seven-year waiting game," Mr. Rangasayee says.

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## Companies within this Article

Altera Corp.(ALTR)	25.36	-0.21	2:20p.m.
Intel Corp.(INTC)	22.12	-0.12	2:20p.m.
Archer Daniels Midland Co.(ADM)	29.02	-0.08	2:20p.m.
SanDisk Corp.(SNDK)	33.00	-0.29	2:19p.m.
Xilinx Inc.(XLNX)	27.01	-0.30	2:20p.m.

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