



## News Analysis [More News Analysis](#)

### Most Recent Comment

Critical detail: How many SERDES are on this chip? And how fast do they run? That's the first question I ask when looking at FPGAs.

**tsat**

## Startup Applies Spacetime to FPGAs

MARCH 1, 2010 | Craig Matsumoto | [Comments \(5\)](#)

[Post a Comment](#) | [Print](#) | [Reprint](#) | [Share](#) | [Email This](#) | [RSS](#)

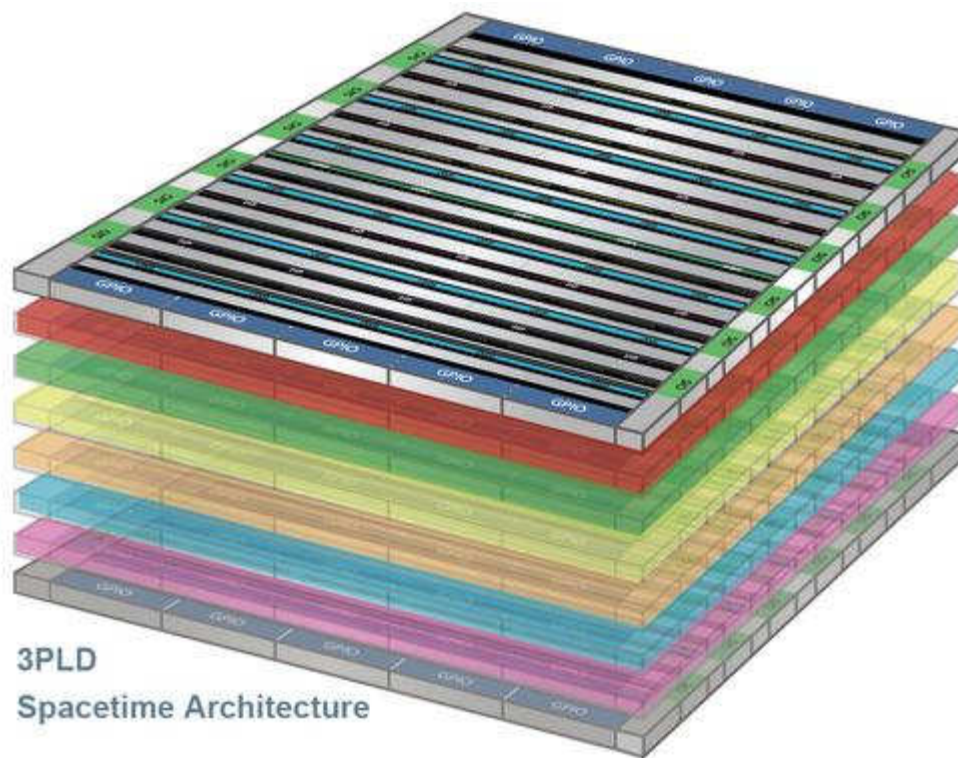
It's a longstanding tradition in semiconductors that any programmable-logic startup gets chewed up and fed to the fishes. That hasn't deterred a handful of startups, and one of them, [Tabula Inc.](#), came out swinging today. (See [FPGA Graveyard](#).)

Tabula produced test samples of its first chips three years ago and now has them in the hands of some customers. But it's only now that the company is revealing why it thinks its devices can upend the [Application-Specific Integrated Circuit \(ASIC\)](#) and [Field Programmable Gate Array \(FPGA\)](#) worlds.

Specifically, the startup is gunning for [Altera Corp.](#) (Nasdaq: [ALTR](#)) and [Xilinx Inc.](#) (Nasdaq: [XLNX](#)), the only two vendors that sell high-end FPGAs. Tabula claims its chips will outdo theirs and sell at around the same prices.

Tabula's trick is that its chip can reconfigure itself on the fly, up to eight times per cycle. (The chip's clock runs at 1.6GHz.) The entire chip doesn't have to reconfigure at once. That is, some sections could change eight times per cycle, while others change only once or twice, or not at all.

### The Eightfold Way



The eight chip layers represent different configurations that the chip morphs into over time. Source: Tabula

So, why would that be useful? For starters, in large FPGAs, the interconnects have become a bottleneck; the time it takes for a signal to get across the chip can actually mess up a design. Moreover, FPGAs tend to be slower and more power-hungry than their ASIC counterparts, factors Tabula hopes to overcome.

But the chip could have advantages over ASICs as well.

"To do a custom piece of silicon, by the time you're done with development, the cost can be \$60 million to \$100 million, easy -- and of course development *times* themselves are stretching way out," says Dennis Segers, a former Xilinx executive who is now Tabula's CEO.

In trying to get complex chips to take up less space, the industry has tried making three-dimensional devices -- increasing chip size by adding layers vertically rather than spreading out horizontally. But no viable chips of that type have emerged. Nor would 3D chips necessarily be cheaper than ASICs; they're harder to manufacture.

Tabula's technology, named Spacetime, is a 3D chip in spirit. But rather than stack circuits, Spacetime alters the chip configuration to create the next "layer." These changes work in a cycle, returning the chip to its original state when the next clock cycle starts.

So, where a 3D chip would send a signal up to, say, some memory block on the second layer of the chip, Tabula just reconfigures the chip to put the memory block in a new spot that's right next to the signal.

It sounds confusing. The key to the whole operation is that the chip can be designed as if it *were* 3D.

The engineer doesn't have to know any of this Spacetime or light-cones stuff. "To the user's point of view, the chip looks 3D," says Steve Teig, Tabula's president and CTO.

Moreover, Tabula's tools -- the software that engineers use for creating chip designs -- mimic the familiar design processes of FPGAs and ASICs today. That could be huge. In some cases, programmable-logic startups tried to get users accustomed to a different design flow, using unfamiliar software tools. With Altera and Xilinx dominating the market, that approach doesn't work.

"It's about the tools. People basically use Altera and Xilinx tools," says Rich Wawrzyniak, an analyst with [Semico Research Corp.](#) .

This is where Tabula thinks it's got a critical advantage over history's other FPGA wannabes. Teig, who founded the company, comes from the software side of the industry, having previously launched two electronic design automation (EDA; i.e., *tools*) companies.

Among his past accomplishments is another parlor trick for chip designs: With startup Simplex Solutions, he pioneered diagonal on-chip wiring, also known as the [X Architecture](#). It helped Simplex get [acquired by Cadence Design Systems Inc.](#) in 2002.

Officials are hoping to make Tabula into the next big franchise in its field; Segers has visions of the company taking a permanent place alongside Altera and Xilinx.

But it's taken money, to the tune of \$100 million in funding in three rounds so far. "Building a semiconductor company these days, especially at advanced processes, is an expensive gig," Segers says. "We have deliberately pursued financiers who understand that, who understand that we're trying to build a large, sustainable, multibillion-dollar company."

Those investors include [Benchmark Capital](#) ; [Balderton Capital](#); [Crosslink Capital](#) ; [Duff Ackerman & Goodrich LLC \(DAG\)](#) ; [Greylock Partners](#) ; [Integral Capital Partners](#) ; [Lighthouse Capital Partners](#) ; [New Enterprise Associates \(NEA\)](#) ; and [SVB Capital](#).

It's taken patience, too. Tabula has had chips for three years, the first samples having come off the fab line in 2007. Part of the wait has been due to Tabula's choice of advanced manufacturing processes -- 40nm line widths, for chip geeks -- that were still in an early, experimental stage at the time.

Wawrzyniak has followed the FPGA industries for years and is aware of its trail of dead startups. But he thinks Tabula has a shot. "This appears completely different from anything else anybody has ever done, as far as I know," he says.

What's particularly intriguing, he adds, is that Tabula doesn't have to stick to the communications industry, or even to FPGA/ASIC replacement. Spacetime could be used to create a microprocessor that boosts performance by more efficiently accessing memory, for instance. "I think it can be applied to other kinds of devices besides FPGAs. That starts to be interesting," Wawrzyniak says.

— Craig Matsumoto, West Coast Editor, [Light Reading](#)

[Post a Comment](#)   [Print](#) | [Reprint](#) | [Share](#) | [Email This](#) | [RSS](#)

Copyright © 2010 TechWeb, A UBM Company, All rights reserved.