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Xilinx banks on power efficiency for 28-nm

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SAN FRANCISCO—By the end of this year, Xilinx Inc. will begin sampling 28-nm FPGAs that consume half the power of its current devices while offering twice the capacity as previously possible, the company said Monday (Feb. 22).

To address issues in static power leakage and overall power management, [Xilinx](#) (San Jose, Calif.) will use a high-performance, low-power process technology in manufacturing at the 28-nm node, a departure from the company's previous approach. Also, for the first time, Xilinx will use a common, scalable architecture across its Virtex and Spartan product lines at the 28-nm node to facilitate easier customer migration between the products.

"At the 28-nm node, we are using low power, high-performance process technology," said Suresh Menon, vice president of product development for Xilinx' programmable platforms development group. "That's very different from the choices we have made in the past. It's also very different from the choices that our competitors make."

Menon said static power leakage is becoming a more critical issue at each technology node. Past scaling drove both performance and power consumption improvement, he added.

"That has certainly changed," Menon said. "We hear from nearly every customer about power these days. They'll tell you they want half the power but they also want more performance."

Rich Wawrzyniak, an analyst with Semico Research Corp., said it is important for Xilinx to address the power consumption issue. "The real problem is, we've been spoiled for years," Wawrzyniak said. "When we move to next process geometry, we've been able to increase transistor count, reduce power and increase performance. We've gotten used to that. But given the sheer number of transistors on these devices and leakage issues, now it becomes a big issue."

Xilinx plans to use Taiwan Semiconductor Manufacturing Co. (TSMC) and Samsung Electronics Co. Ltd. as its foundry suppliers at the 28-nm node. The company, which has long maintained a two-foundry strategy, has used TSMC rival's, United Microelectronics Corp., as a foundry supplier for more than a decade.

Using a high-k metal gate, high-performance, low-power process technology delivers that are 50 percent lower in static power compared with those produced on a standard high-performance process, according to Xilinx. The lower static power contributes to a 50 percent reduction in total power compared to previous generation devices, the company said. Xilinx is offering new development tools partial reconfiguration technology that the company says further reduce power consumption.

Xilinx said it also plans to provide performance interfaces to support customers who need high-bandwidth chip-to-chip, board-to-board and box-to-box connections. According to the company, this will make it easier for customers to build systems based on FPGAs when ASIC and ASSP options are unavailable.

Offering samples of 28-nm devices by the end of 2010 could help Xilinx narrow competitor Altera Corp.'s edge in process technology migration. Altera has said it would have 28-nm chips available in 2010, but has not provided a more specific target.

Unifying the ASMBL architecture of its products furthers Xilinx' goal of "socketable IP," allowing customers to move IP from one platform to the other, according to the company.

"That's a really big deal," Wawrzyniak said. "People are spending a lot of time and money and effort on IP these days. Any lessening of the amount of effort they need to expend to carry their own IP forward is a big plus."

Xilinx said it plans to offer initial 28-nm devices in the fourth quarter of the year. Initial tool support from the company's ISE Design Suite is expected in June, Xilinx said.

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