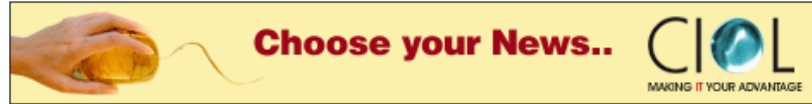


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Altera planning innovations for its first 28-nm chips

The innovations include partial reconfiguration, embedded hard intellectual property (IP) blocks, and 28-gigabit-per-second (Gbps) transceivers

Tuesday, February 02, 2010

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SAN FRANCISCO, USA: [Altera](#) Corporation, the vendor of FPGA, based in San Jose, California, the United States, has said it plans to introduce a number of innovations for its first 28-nm chips.

The innovations include partial reconfiguration, embedded hard intellectual property (IP) blocks, and 28-gigabit-per-second (Gbps) transceivers.

In a statement, Altera Corporation said it intends to make available 28-nm FPGAs available in 2010, without disclosing the exact date of their introduction.

The company said the partial reconfiguration capability on its 28-nm chips will allow customers to load new functionality into portions of the FPGA, without interrupting normal operation. Users, Altera Corporation stressed, will profit from reduced cost and electricity consumption by implementing only active logic.

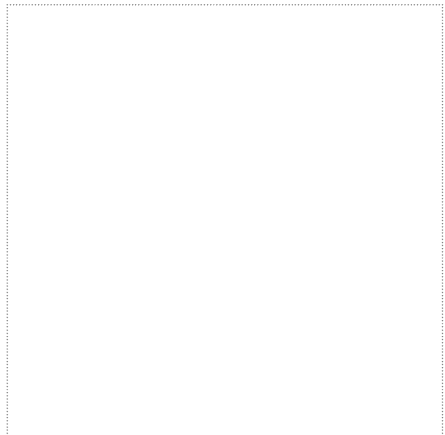
Also, partial reconfiguration on its 28-nm chips will all enable users to implement system enhancements remotely, without affecting the operations of the FPGAs, Altera Corporation claimed.

Luanne Schirrmeister, senior director (product marketing) of Altera Corporation, explained in the statement that though partial reconfiguration is not a new concept, this is the first time that the company has attempted to offer partial reconfiguration.

Rich Wawrzyniak, an analyst with Semico Research Corporation, termed Altera Corporation's partial reconfiguration technology as a "real step forward" for the programmable logic sector.

At present, Altera Corporation offers what it claims to be the fastest transceiver available on an FPGA.

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