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Altera to offer partial reconfiguration at 28-nm

28-Gbps transceivers, embed hard IP also on slate

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SAN FRANCISCO—FPGA vendor Altera Corp. plans to introduce several innovations for its first 28-nm chips, including partial reconfiguration, 28-gigabit-per-second (Gbps) transceivers and embedded hard intellectual property (IP) blocks, the company announced Monday (Feb. 1).

[Altera](#) (San Jose, Calif.) has said it intends to have 28-nm FPGAs available this year. However, the company has not disclosed a specific target date for their introduction.

According to Altera, the partial reconfiguration capability on its 28-nm chips will enable customers to load new functionality into portions of the FPGA without interrupting normal operation. Users will benefit from reduced cost and power consumption by implementing only active logic, the company said. Partial reconfiguration will all enable customers to implement system enhancements remotely, without disrupting the FPGA's operation, the company said.

Luanne Schirrmeister, senior director of product marketing at Altera, said partial reconfiguration is not a new concept, though this is the first time Altera has attempted to offer it. It's never really gained much traction, Schirrmeister said, partly because using it required customers to learn all the intricate architectural details of a device.

"What we are going to do that is different," Schirrmeister said. "We are going to built partial reconfiguration as a natural extension of our functional design flow." The capability will be built on top of the incremental compile design flow in its Quartus II design software, she said.

Rich Wawrzyniak, an analyst with Semico Research Corp., described Altera's partial reconfiguration technology as a real step forward for the programmable logic market. "Yeah, it's going to require people to really understand their application and think long and hard about what they are going to do," Wawrzyniak said. "But if you can do that, what they've provided here is going to allow people to come up with some real innovative stuff."

Xilinx Inc. has ofered a technology called active partial reconfiguration on several of its FPGAs.

The customizable hard IP blocks that Altera will enable customers to use at 28-nm are embedded HardCopy blocks that customizable and utilize the capabilities of Altera's HardCopy ASICs, the company said. Altera's HardCopy ASIC technology.

Altera said it has also developed 28-Gbps embedded transceivers that will enable customers to implement next-generation designs such as 400G systems on a single chip without the need for external components.

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