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When It Comes To Intellectual Property, Size Matters

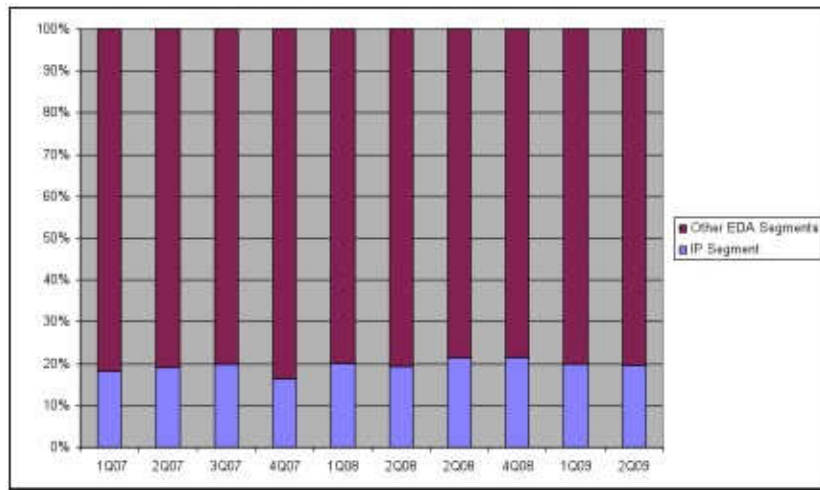
By Geoffrey James

Intellectual property was once seen as the new growth market for EDA. Dozens of firms – large and small – jumped on the IP bandwagon, attracted to the “build once, sell many times” business model.

“As late as 2004, the industry was still thinking that as much as 90% of SoCs would be reused IP,” said EDA consultant Gary Smith.

The IP segment, however, hasn’t proven to be a profitability panacea, especially for smaller firms. There are the big players—Synopsys and Mentor in the EDA world, ARM and MIPS on the processor side, and Virage Logic in a variety of markets, which has broadened recently with the acquisition of ARC and NXP’s IP portfolio. There also are players like Rambus and Denali that have staked out strong market presence. For most other companies, though, IP has been more troubling than it has been worth, as evidenced by the continued consolidation in this sector.

For one thing, IP never achieved the promised level of penetration. Reusable blocks comprise only a little more than two-thirds of today’s typical SoC, according to Smith. Perhaps as a result, since 2007, IP revenue has stalled at or around 20% of total EDA market. (See figure 1.)



Source: EDAC

But there have been other problems as well, especially for smaller firms. Far from an easy way to make money, IP has become one of the most harrowing segments of the EDA market, with five major financial and technical challenges:

CHALLENGE #1: New IP always requires customization.

Back when IP first became big business, state-of-the-art circuitry was around 180nm. At those geometries, IP was pretty much plug and play. If a block of RTL did something on one chip, it would do the same thing on another chip. While the overall chip had to use the block correctly, there wasn't much else that could go wrong. It didn't matter what foundry made the chip, nor what other kinds of circuits were in the general vicinity of that particular block of IP.

That all changed at around 90nm. Suddenly, a circuit that worked perfectly on one chip would go all catawampus on another, simply because of leakage from surrounding circuitry. Even the same chip manufactured at different foundries might end up with wildly different yields, due to the peculiarities of the individual processes. As a result, IP, if it's complicated or if it's targeted for the smallest geometries, stops looking "plug and play" and starts looking like custom design work.

This screws up the "build once, sell many times" business model, says Smith. "Design firms selling state-of-the-art IP often find themselves spending more time tuning the blocks for specific designs than creating new IP to sell," he says. In order to survive, smaller IP firms must extract revenue from the customization, rather than from the IP license. Unfortunately, this ties up their most precious resource—top engineering talent—thereby limiting their ability to continue to innovate.

CHALLENGE #2: New IP has a short market window.

Once a certain type of IP is well-understood and has been qualified for multiple manufacturing processes, it does begin to approach the plug-and-play status that would make "build once, sell many times" workable. However, once the IP reaches that state, it's generally no longer unique enough to command a premium price. Instead, there will be multiple plug-and-play approaches to solving that problem. The IP becomes a commodity, making it more difficult to recoup the development expense.

For example, when USB 2.0 first came out, the IP to make it work commanded a premium license fee. However, once USB 2.0 had gone into enough designs, the problems making it work with different processes were largely solved and easily imitated. Because of that, chip designers can choose from a number of different versions of USB 2.0 IP and since none of them are noticeably better than the other, semiconductor firms are likely to pick the cheapest.

That's probably OK, if you're selling a knockoff. But if you invested a lot of time and money to come up with the first version, and then qualify it on multiple processes, you have a very limited amount of time to obtain the kind of high license fee that would provide a good return on that development investment, according to Richard Wawrzyniak, ASIC and SoC senior market analyst at Semico.

"The IP world is driven by your ability to differentiate your customer's product," he says. "If you can't provide that differentiation, then your IP has limited value."

CHALLENGE #3: IP Litigation can get expensive.

With chip designs costing more money every year, it's not surprising that many semiconductor firms are outsourcing designs to India and China, where engineers are plentiful and cheap. Unfortunately, China (and to a lesser extent India) has an abysmal record of protecting high tech IP. "The entire idea of intellectual property is alien to Chinese culture; China didn't even have

patent laws until 1990,” explains Usha Haley, a business school professor at the University of New Haven and author of *Asia’s Tao of Business: the Logic of Chinese Business Strategy* (Wiley, 2004).

Unfortunately for their profitability, IP firms can find themselves involved in legal hassles related to the unauthorized use of their IP. That’s just a cost of doing business for large IP firms. Smaller IP firms, however, simply can’t afford that expense, according to Charlie Cheng, CEO of Kilopass, a company that holds IP patents for non-volatile memory. “Our only defense is to keep innovating so that people will keep doing business with us rather than stealing our IP,” he explains.

CHALLENGE #4: Semiconductor firms want to manage their risks.

Many semiconductor firms look a bit askance at IP because it makes them dependent upon the IP supplier. If something goes wrong with the IP during, say, verification or manufacturing, the IP supplier might not be willing (or able) to drop everything and run to fix the problem. And if the semiconductor firm hopes to move a chip design to a newer node, the IP supplier may need to get re-involved and possibly retrained on the design rules for a new process.

Under the circumstances, many semiconductor firms prefer to develop as much as possible of their circuitry in-house, so that they have control over development priorities if a problem occurs. Many firms only turn to IP when they lack the expertise to develop an in-house product. CPU IP is a case in point, according to Art Swift, vice president of marketing at MIPS. “We’ve been working on the RISC computing concept for decades, which has created a vast experience base and intellectual process that would be difficult, if not impossible to reproduce elsewhere,” he explains.

In other words, smaller IP suppliers entail risk that some semiconductor firms aren’t willing to suffer, according to George Zimmerman, chief technical officer at Solarflare, a company that makes 10 Gigabit Ethernet chips and controllers. “Going with a larger firm offers more risk mitigation,” he says. “We’ll only work with a smaller IP firm when what we need is highly specialized and can offer a substantial performance advantage.”

CHALLENGE #5: IP design favors economies of scale.

In contrast to their smaller brethren, the larger IP vendors have more resources to apply to making sure the IP behaves as expected. Synopsys is a case in point. “We have about 700 people working in our IP group who focus on adapting IP to run on different process nodes and for different customers,” says John Koeter, the company’s vice president of marketing for the solutions group. This massive application of manpower allows Synopsys to achieve the “build once, sell many times” business model.

Smaller firms, however, lack the economies of scale to imitate Synopsys’s success. Instead, they’re forced to marshal whatever resources they can to help a handful of customers, most of whom will require a significant amount of custom work. And while that still is revenue, it’s not as easy as getting a check every month for your IP licenses.

This is not to say that smaller firms can’t make money in chip IP, according to Smith. “The ones doing OK are making analog content because analog is difficult and there aren’t analog engineers available to be hired,” he says. But the idea that IP could be a short cut to big money for small firms remains a dream unfulfilled. “The reality is that it’s just not as easy as it looks to make money in this business,” Koeter says.

The barrier to entry also has escalated well beyond what it was at 130nm or even 90nm. The companies looking for IP typically are at the leading edge of design, which means the IP has to be qualified and tested for that process node.

“Prior to 45nm, there was no IP ready before silicon, said Brani Buric, vice president of marketing and strategic foundry relationships at Virage Logic. “Now you have to design complicated technology for SoCs, test it and verify it. So the skill level required on a scale of 1 to 10 went from 3 to 20. It’s tough to be a small player in this market.”

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