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## MIPS debuts new cores, instruction set

Designs aim to expand controller, wireless reach

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SAN JOSE, Calif. — MIPS Technologies Inc. is upgrading two of its cores and introducing a new instruction set architecture. The products aim to expand the company's relatively small presence in 32-bit microcontrollers and leverage its strength in wired consumer systems to attack sockets in wireless devices.

MIPS disclosed details of a new M14K core, an upgrade of its M4K core for microcontrollers and a new M14Kc core, an upgrade of its M4KE used in more sophisticated consumer systems. Both support as an option a new microMips instruction set that the company claims provides 32-bit performance at 16-bit code compression levels.

The company is hungry for growth. Its revenues flattened, royalties declined and profits largely evaporated since 2007. In its most recent quarterly results announced last week, MIPS did eke out a small profit and see revenue growth from the prior quarter, albeit still down from a year ago.

"We are optimistic that we have passed the low point in revenues," said John Bourgoin, MIPS chief executive, in a prepared statement at that time.

The 14K core, and the promise of a 35 percent reduction in code size using the new microMips instructions, could help the company ride a wave of expected growth in the 32-bit microcontroller market. Semico Research (Phoenix) forecasts the microcontroller market overall will see 14.9 percent growth next year and the 32-bit slice of it will jump 30.3 percent from 2009.

Today MIPS has a market share measured in single digits for the highly competitive 32-bit controller market thanks to its licensees MicroChip, NEC and Toshiba. Those three companies--along with Renesas, Freescale and Infineon—dominate the microcontroller market with mainly proprietary architectures today.

Like MIPS, ARM also aims to replace many of those proprietary controllers with standard products. ARM already has about a 25 percent market share in controllers according to Semico thanks to designs based on its M3 and other cores.

MIPS "needs to expand in the 32-bit microcontroller area, and the code compression will be a critical element helping them with that," said Tony Massimini, a senior analyst with Semico.

The new cores sport the same pipeline structure as the parts they replace, but they include decoders for both existing MIPS 32-bit and the new microMips instructions. MIPS's existing 16-bit instruction set offered code compression but performance fell below 32-bit levels.

Eight software companies said that will support the microMips instruction set, although none announced when they will have products ready for it. They include RTOS and Linux operating system providers such as ExpressLogic, Mentor Graphics, Micrium and Montavista as well as tool providers such as CodeSourcery, Carbon Design and Imperas.

MIPS is sampling early versions of the cores to partners before the end of the year. General availability is expected before April, and chips using the cores likely will roll out in 2011.

The M14K is generally targeted at use with flash memory. The 14Kc has a full memory management unit with translation look-aside buffer needed to support virtual memory and thus run full operating systems such as Linux and Android.

Both cores reduce interrupt latency to about 21 cycles, down from 30 cycles, thanks added hardware and new software, enhancing real0-time performance. In addition, the 14K sports a pre-fetch buffer to accelerate flash performance as much as four times over the previous generation.

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