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The FPGA Alternative

By Geoffrey James

Until a few years ago, SoC designers focused almost exclusively on ASICs. While it was theoretically possible to create an SoC design for an FPGA, the programmable chips were too bulky and pricey to be useful for much more than prototyping. Today, however, designers are increasingly turning to FPGAs for their SoC targets for production systems.

Why the sudden upsurge in SoCs on FPGAs? The answer, as usual, is Moore's Law – and the design hassles it creates. ASIC designs at sub-65nm are becoming increasingly expensive to develop. And turning an ASIC design into physical silicon can take months, so if there's a design flaw that's elapsed time that could mean missing a market window. By contrast, FPGAs offer SoC designers the flexibility to tinker and test without the expense and risk of a manufacturing run.

Even so, there's more than economics at play here. Four key technical trends have conspired to make FPGAs more viable as a platform for serious SoC production.

Trend #1: Today's FPGAs are gaining features appropriate for SoCs.

In the past, FPGA were often implemented as an element in a larger chip set that would be integrated on a board. Standard functions were relegated to other (smaller) chips, while the FPGA (which was hefty by comparison) carried the part of the design unique to the end product. This tended to make FPGA designs expensive because the FPGA chip was more expensive than a comparable ASIC and the additional chips and assembly added additional design and manufacturing costs.

Today, however, FPGAs are much smaller and more efficient than before. Xilinx, for instance, makes FPGAs at 40nm, while

Actel has developed a 65nm version with flash memory. Though FPGA circuitry still takes up more physical space than non-programmable circuitry, at 65nm and below there is more than enough raw circuitry to support a wide range of designs.

“We see FPGAs as a major vehicle for innovation among our customers, who have used it to develop capabilities that we were later able to incorporate inside our standard products,” says Pranav Mehta, CTO of Intel’s embedded and communications group.

Newer FPGAs also include standard functions such as USB communications, sometimes encapsulated inside “hardened” (i.e. non-programmable) portions of the chip. Some FPGAs even have CPU cores built into them or support special versions of CPU cores (such as an ARM processor) that can run inside the programmable portion of a hybrid FPGA.

“The inclusion of advanced features makes FPGAs strong candidates for even complex SoC designs,” says John Swanson, senior manager of the solutions group at Synopsys.

Trend #2: The FPGA tool sets are becoming more sophisticated.

Programming FPGAs originally involved using rudimentary tool sets provided by the FPGA maker. However, as FPGAs (and the applications on them) have gotten more complex, EDA firms have come to the assistance of designers with better FPGA development tools. Forte Design Systems, for example, provides an ESL design environment that supports FPGAs as effectively as ASICs, according to Brett Cline, the company’s vice president of marketing and sales. “We have one client who is doing seven designs, three of which are targeted at FPGAs,” he explains. “We even have one client who is porting an ASIC design back onto an FPGA for further development.”

The traditional EDA vendors have taken FPGA more seriously over the years because their customers demanded it, according to Daniel Platzker, the product line director for FPGA synthesis products at Mentor Graphics. “While FPGA tools have been around inside Mentor since 1992, it’s become a major market for us in the areas of synthesis, verification and simulation,” he says. (See Figure 1)

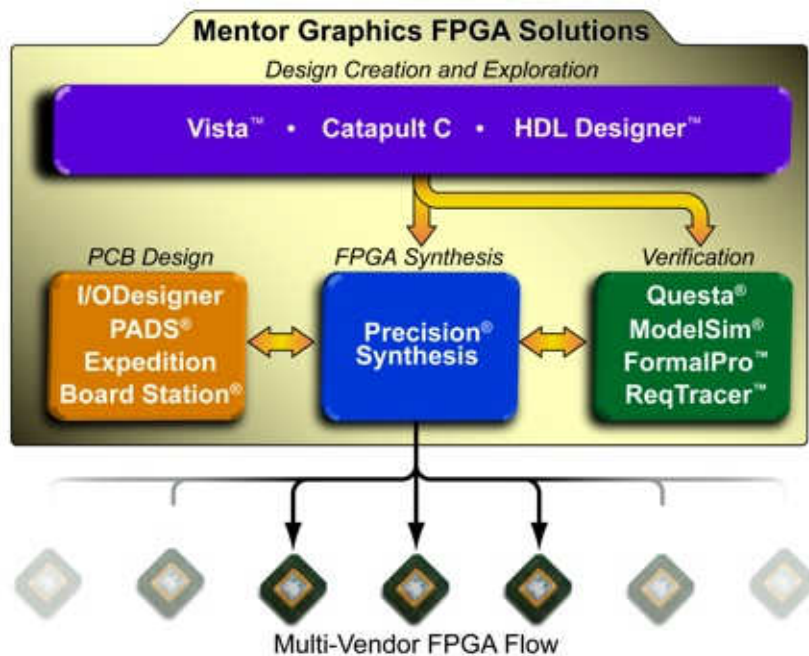


Fig. 1: Mentor Graphics' FPGA design environment.

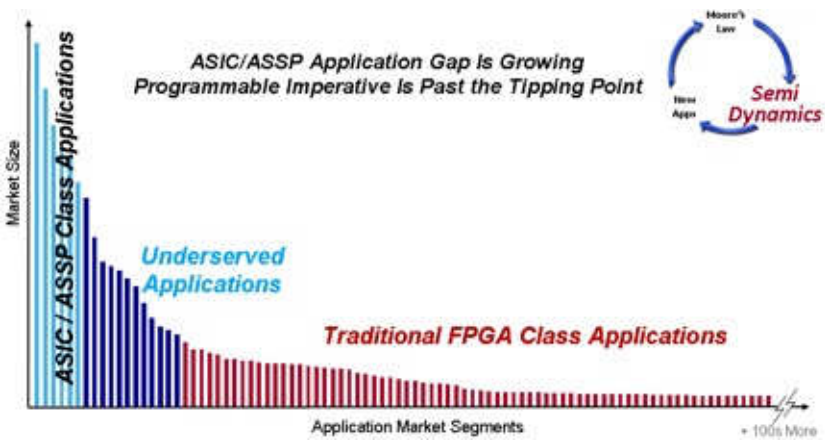
Andy Biddle, director of business development at Magma agrees. “We see even customers using FPGAs to develop mix-signal designs that previously would have been difficult or impossible,” he says.

The demand for better tools was spawned by the fact that newer FPGAs can experience some of the same challenges that occur in ASICs. “These designs get so complex that it’s necessary to have professional-grade routing tools, for instance, to ensure that the chip doesn’t run into any problems with timing and closure,” says Juergen Jaeger, director of marketing, for the Confirma rapid prototyping platform at Synopsys.

Trend #3: SoCs are proliferating into a wider range of products.

As sophisticated electronics get built into an ever-wider variety of devices, it's creating an almost insatiable demand for FPGA-style SoCs. "Designers in third-world countries work in environments that won't support and can't afford a full ASIC development process," explains EDA analyst Gary Smith of GarySmithEDA.com. "In order to save money, they're using FPGAs in everything from vacuum cleaners to fans to pumps."

FPGAs also are showing up in products elsewhere in the industrialized world, according to Tom Feist, senior director of marketing for IP products at Xilinx. "We're seeing substantial FPGA interest in the automotive industry for SoCs that can be easily upgraded to handle new features, like shape recognition and object avoidance," he explains. (See Figure 2)



Relative markets for FPGAs vs. ASICs

Given the wealth of potential markets, it's probably not surprising that the number of FPGA design starts dwarf the number of similar ASIC design starts. "There are 140,000 FPGA designs done every year as opposed to 10,000 to 12,000 ASIC starts," says Rich Wawrzyniak, senior analyst at the market research firm Semico. While he counsels that only 5% of those FPGA starts end up in finished products, that's still an enormous amount of SoC development.

Trend #4: Converting from FPGA to ASIC is constantly getting easier.

Targeting an SoC design at an FPGA platform is a cost-effective way to develop a product. Typically, companies use the FPGA in the new product until it becomes clear that product volumes will be large enough to justify an ASIC version of the chip. "The FPGA has come a long way in terms of the fundamental hurdles of unit cost and power utilization," says Intel's Mehta. "But there's still no question that for large volumes, ASICs will continue to remain more economic."

Fortunately, it's becoming easier than ever before to re-target an SoC design from an FPGA to an ASIC. Forte, for example, supports two design trees from the same code base, allowing chip designers to target both platforms. "We encourage designers to think about their designs at a higher level, without being forced to worry over much about whether the final chip is programmable," says Cline.

The use of an FPGA in early development phases can reduce overall costs at the corporate level because the lower cost lowers the risk of a product failure. "FPGAs allow you to more easily hit a market window, thereby making it more likely that you'll have a hit product," explains Synopsys's Jaeger. And because the door is open to move the design to an ASIC, if and when the time is right, it's no wonder FPGAs are proving so popular among the SoC-savvy.

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