

[Advanced Search](#) [All Recent News](#) [Email a Friend](#) [Print-Friendly](#)

**SOURCE: Cadence Design Systems, Inc.**



Jun 08, 2009 08:00 ET

## **Cadence Unveils Integrated Chip Planning and Implementation Solution to Improve Predictability and Reduce Risk of IC Designs**

### **New Breakthrough Approach Provides Visibility Throughout Design Process From IP Selection to Implementation and Signoff**

SAN JOSE, CA--(Marketwire - June 8, 2009) - Cadence Design Systems, Inc. (NASDAQ: [CDNS](#)), the leader in global electronic design innovation, today unveiled a breakthrough solution that provides design and implementation engineers with superior visibility and predictability of chip performance, area, power consumption, cost, and time to market across the full range of design activities, including system-level design and IP selection through final implementation and signoff. This unique and automated approach to semiconductor design has been achieved through the integration of [Cadence® InCyte Chip Estimator](#) and the [Cadence Encounter® Digital Implementation \(EDI\) System](#) technologies. The combination of these technologies increases the predictability of key metrics from design specification through final implementation while reducing overall IC project risk.

**Highlighted Links**

[Cadence Homepage](#)

"As development costs of complex SoCs continue to skyrocket, manufacturers in all sectors are looking for increased visibility into their design processes," said Richard Wawrzyniak, senior ASIC/SoC analyst at Semico Research Corporation. "By integrating capabilities from these two products, Cadence addresses a growing industry need by offering a solution that provides a unique and timely window into the development of a SoC."

Decisions made during the architectural planning stages of the design cycle largely determine the chip's resulting size, power consumption, performance, and cost. During these early stages design teams can realize the biggest benefits by considering and quantifying a variety of architectural and IP options prior to final design, implementation and signoff. Traditionally, however, semiconductor designers have been forced to use a manual or disconnected approach to make estimations and architectural choices without the benefit of flexibility, automation, accurate analysis, or tight links to implementation tools. This new Cadence solution eliminates guesswork and provides a new data-driven and holistic approach to the optimization of IP selection and integration through architecture, design, implementation and signoff.

Using the new Cadence solution, designers can quickly and accurately estimate die size, power and cost, including real-time IP and manufacturing process what-if analysis to ease IP selection and determine design architecture and feasibility. As a milestone in Cadence's open, multi-vendor approach to IP, the solution leverages the vast ecosystem of IP at the [ChipEstimate.com](#) portal where over 200 IP suppliers and foundries contribute data to enable this accurate what-if analysis capability. Once system-level trade-offs and architecture are complete, designers can dynamically progress to the final implementation phase, leveraging estimates as a seed and driving to faster convergence. Cadence's EDI System completes the implementation and signoff of the design while monitoring and tracking aspects of block and full-chip progress, and also providing in-situ updates to actual die-size, power consumption, performance and cost with full transparency to all stakeholders. As optimizations in EDI System improve yield, size or power, users can immediately quantify those benefits in terms of the fully packaged chip cost.

"This new solution offers a unique new advantage to semiconductor design teams where all parties involved from system-level architects to chip implementation engineers can now make more informed and precise tradeoffs, including technical and economic metrics," said Charlie Huang, senior vice president and chief strategy officer at Cadence. "It breaks down the barriers between both domains for a more transparent and predictive semiconductor development process. This cost-aware design philosophy is a new paradigm for design teams and addresses the critical market need of cost and risk reduction in IC designs."

The new design solution will be demonstrated at the Design Automation Conference in San Francisco this July and be available later this year.

#### About Cadence

Cadence enables global electronic design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence software and hardware, methodologies, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products, and services is available at [www.cadence.com](http://www.cadence.com).

Cadence, the Cadence logo and Encounter are registered trademarks of Cadence Design Systems, Inc. in the United States and other countries. All other trademarks are the property of their respective owners.

For more information, please contact:  
Dean Solov  
Cadence Design Systems, Inc.  
408-944-7226  
[dsolov@cadence.com](mailto:dsolov@cadence.com)

[Click here to see all recent news from this company](#)

---

[Privacy Statement](#) | [Terms of Service](#) | [Sitemap](#) | © 2009 Marketwire, Incorporated. All rights reserved.  
Your newswire of choice for expert news release distribution.  
1-800-774-9473 (US) | 1-888-299-0338 (Canada) | +44-20-7562-6550 (UK)