



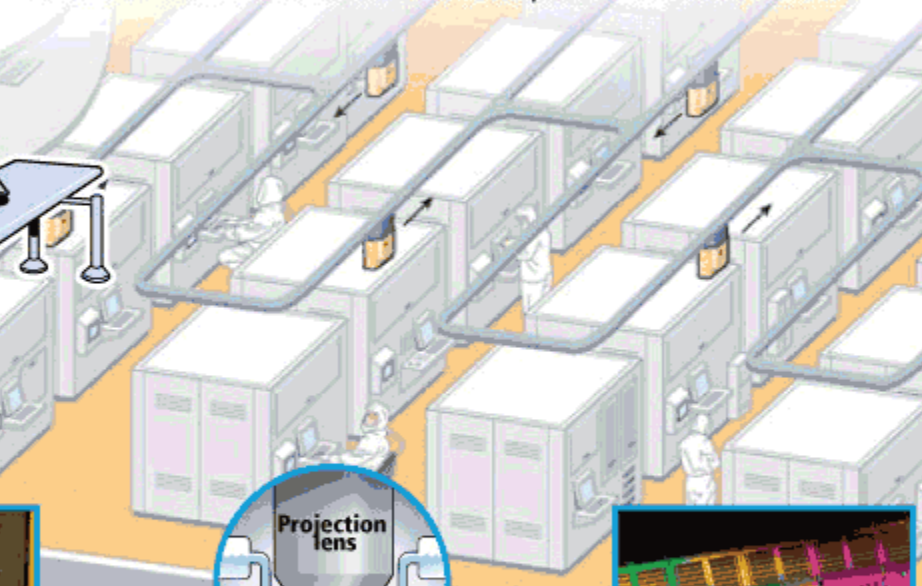
Chips Ahoy

Stimulating Tech

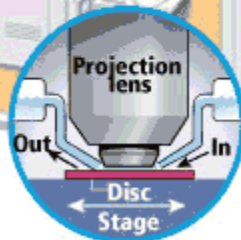
Brian Caulfield, 02.10.09, 3:45 PM ET

HONEY, I SHRUNK THE PROCESSORS

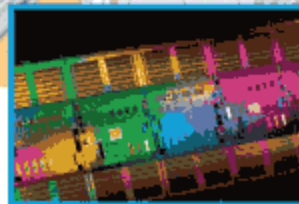
Intel's factories, or fabs, are scattered throughout the world, but they all work the same way. Intel's "copy exactly" methodology is aimed at helping Intel produce processors at one fab as reliably as at any other even as it shrinks the transistors on its chips to 32 nanometers wide.



IN THE FOUP The Front Opening Unified Pod (FOUP) shuttles wafers from one tool to another.



GETTING LIQUID Immersion lithography adds a layer of liquid to traditional lithography to help Intel etch 32-nanometer-wide transistors with light that has a wave of 193 nanometers.



FINAL PRODUCT Intel will put chips made with its latest process into mainstream PCs and notebooks first.

BURLINGAME, Calif.--The march of technology waits for no business cycle. Or so believe the folks at Intel, who plan to pour roughly \$7 billion over the next two years into building factories in the U.S. that will make the next generation of computer chips.

The timing is awkward. In January, Intel announced a miserable quarter, with sales down 23% (to \$8.2 billion) and operating income down 49% (to \$1.5 billion) from the corresponding period a year ago. The market for pcs is shriveling. Intel's shares have fallen 27% to \$14.69 over the past year.

Even so, Intel Chief Executive Paul S. Otellini had a succinct answer when asked if Intel will scale back its construction plans if the company's stock price drops more: "Nope."

Intel is counting on efficiency gains from squeezing transistors together so tightly that a billion fit on a fingernail-size chip. Those gains take two forms: less electricity consumption and a lower cost per unit of processing power. A transistor's components will measure 32 nanometers across, 71% of the size of today's 45-nanometer circuits.

Tiny chips must be made in big spaces. In Oregon, Intel will convert a development factory (with test runs) into a high-volume production factory. In Arizona, Intel will turn two factories into a single one that has a 320,000-square-foot clean room. That's about the size of the Acropolis of Athens. A New Mexico plant will also get a redo to become the world's largest "class-one" clean room, with no more than one 0.5-micron speck of dust per cubic foot.

Inside those arenas, the key to building the next generation of tiny chips is a technique known as immersion lithography. To understand how it works, it helps to know how chips are etched onto silicon. Silicon wafers are covered in a chemical brew called "photoresist." Light is beamed at the wafer through a photo mask carved with parts of the circuit design. Where the light touches the resist, the chemicals turn gooey and can be washed away. Where there is no resist, acids etch away silicon dioxide in the next step. The sculpted layer becomes the foundation for yet another step. More layers of silicon dioxide and other materials are grown on the etched layer. The process then gets repeated, over and over.

These days, the wavelength of light used starts out at 193 nanometers. To avoid heading into the twilight zone of extreme ultraviolet lithography (or, worse, X-rays), chipmakers need to shrink the light.

A layer of water is placed between the lens on the lithography equipment and a silicon wafer. The liquid acts as an additional lens, narrowing the beam of light just as a telescope turns what looks to the naked eye like a smudge on the horizon into a crisp image. That lets chipmakers squeeze smaller, more densely packed features onto the chip.

Of course, doing this on the factory floor is tricky business. In 2000 and 2001, as the industry switched to 12-inch wafers from eight-inch ones and to processors with features 0.13 microns (130 nanometers) wide from 0.18 microns, chipmakers were hobbled by delays, says Joanne Itow, managing director of manufacturing research at Semico Research.

Intel thinks it has nailed the 32-nanometer process: It reports that defect rates for the first chips in its development factories are comparable to what it saw when it switched to 45-nanometer technology two years ago, a transition that went smoothly. "The very first wafers that came out of the fab produced chips that could be booted in systems," says Intel senior fellow Mark Bohr. "We were all very surprised and excited."

When Otellini heard the news, he told his assistant to get one of the new processors in a PC, pronto. Otellini then used it to serve up the PowerPoint slides during a presentation to Intel's sales force on Jan. 18. "Halfway through my speech I told them, 'Oh, by the way, this entire presentation is running on Westmere,'" the provisional name for Intel's first round of processor chips etched at 32 nanometers. The throwaway line got a standing ovation.

Immersion lithography has been used in production since 2004, but Intel will be pushing this technology to the extreme. Rival chipmakers switched to immersion lithography before Intel did. Intel deferred the day of reckoning by using other tricks to shrink circuit sizes.

Still, the dollars Intel has to lay down on the table spell big risk: about \$1 billion for grunty stuff like cement, labor, pipes and air filtration systems. New tools will cost \$1 billion to \$2 billion per fabrication plant. Apart from temporary construction crews of 4,200 to 4,700 people, however, the spending won't mean new jobs. Instead, about 7,400 Intel employees will simply stay employed, along with 4,500 contractors. The production lines should start running in a limited way by the end of 2009 and full-out in 2010. Then Intel needs to sell all those new chips.

In the past Intel has first put its newest process technology to work in pricey server processors and chips for high-end gaming machines. This time, the new chips will go straight into mainstream desktop and notebook machines.

Otelchini offers a geeky rationale: "One of the best ways to use this kind of capacity is for what I call a 'square-wave transition,' to bring massive amounts of new technology at a great price point," he says. (A square wave is how an electrical engineer thinks of an abrupt transition.)

Translation: If you're willing to plunk down a few bones on a new computer at Best Buy next year, you're going to get something better, for less, than you could before. Now, that's a stimulus package.

See Also:

[Intel's Stimulus Plan](#)

[Intel Chief On His \\$7 Billion Bet](#)

[Intel's Tough Quarter](#)