

## Flurry of Floating-Body Memory Research, but Still No Products

By **Monica Heger**

6 October 2008—It was seven years ago that two men from Switzerland introduced a new kind of memory. The technology—the [floating-body memory cell](#)—had the potential to produce the most dense form of memory around, as good as doubling the bits stored on a typical DRAM or quintupling the data of SRAM. The introduction came at the [2001 IEEE International Silicon-on-Insulator \(SOI\) Conference](#). Today floating-body memory is again on the agenda at the SOI conference, which began this week in New Paltz, N.Y. But a lot of things have changed since 2001. Those two men from Switzerland founded a memory company, Innovative Silicon, that has made multimillion-dollar licenses of their technology to processor maker Advanced Micro Devices and to DRAM giant Hynix Semiconductor. And they've been joined in their quest to develop floating-body memories by competing research teams at such heavyweights as Toshiba and Intel, both of which are reporting new research in New Paltz this week.

Despite the two big-name licensees—AMD in 2006 and [Hynix in 2007](#)—so far no product with Innovative Silicon's Z-RAM technology or any other floating-body technology has yet emerged. Yet floating-body memory's prospects are in no way dead. In fact, a number of factors suggest that it is more likely than ever to be adopted.

Patents for the technology jumped from 41 to 110 between 2005 and 2007, according to Innovative Silicon, and the number of published studies increased from 39 to 68 in the same time frame. Meanwhile, research and business deals in the past two years have expanded the technology's usefulness beyond embedded memory in processors and systems-on-a-chip made on specialty, SOI wafers. Now there's a possibility that it could work for chips made using ordinary "bulk" silicon and for stand-alone DRAM memory chips—the typical memory found in all sorts of computers.

In addition to Innovative Silicon's activities, Toshiba has been working on its own version of floating body memory and is presenting new research this week. Two years ago, the company told IEEE Spectrum of plans to license its technology but has kept mum since then and would not answer questions for this article. Intel has also persistently pursued the technology. It is presenting work this week on floating-body cells built using the 16-nanometer features needed for chips in the next decade.

In whatever form the floating-body memory first appears, Jeff Lewis, Innovative Silicon's senior vice president of marketing and business development, predicts the first product to incorporate it will be out in 2009 or 2010. Innovative Silicon's CEO, Mark-Eric Jones, says that floating-body memory has just as high a chance of being produced as stand-alone DRAM as it has as embedded memory. "I would be hard pushed to say which one will be in production first," says Jones.

Floating-body memory is a technology that some think will be the answer to problems with both DRAM and SRAM—the memory found on processor chips themselves. A DRAM cell consists of a capacitor, which stores the bit as charge, and a transistor. It's the capacitor that has become the problem. While transistors follow Moore's Law, becoming steadily smaller with each generation, capacitors don't scale down nearly as well. As the years go by, building DRAM has become more difficult. Floating-body cells, on the other hand, have just a single transistor each, storing the bit as charge within the transistor itself, so they need no cumbersome capacitor.

Having only a single transistor per cell, floating-body memory has a size advantage over SRAM, because each SRAM cell has six transistors. So Innovative Silicon's Z-RAM, for example, packs 5 megabytes of memory into the same space as 1 MB of SRAM.

However, in order to make the transistor work as memory, you have to find a way to temporarily store a bit as a charge inside the transistor. One way to do this is by building the cell on an SOI wafer. The SOI wafer has a thin layer of silicon dioxide a few hundred nanometers below the surface, acting as insulation between the transistor and the rest of the wafer. This insulating layer is important because a transistor produces charge when current runs through it. The oxide layer traps the charge in the transistor, suspending it above the wafer—hence the name "floating body." This floating body of charge can then be used to represent data.

SOI technology has its own set of problems, though. For one, SOI wafers are more expensive. Also, to make chips with SOI wafers requires somewhat different production processes than bulk silicon. Intel is well known for sticking with bulk silicon despite the fact that other processor makers, such as AMD and IBM, choose SOI. "Up to this point, bulk has been the best choice for us," says Mike Mayberry, vice president of Intel's technology and manufacturing group. "While people do make advances, it's a pretty high barrier to adopting it."

Several research groups are exploring methods of making floating-body cells on bulk silicon. Engineers from Stanford University recently developed a memory cell having two gates, instead of the one found in the typical transistor. One gate induces the charge that represents the bit, and the other senses that charge to read the bit. The double-gate cell can easily integrate with existing

bulk silicon technology, says Krishna Saraswat, professor of electrical engineering at Stanford. The design is also scalable and can be shrunk down to have features just 20 nm across.

Intel has also been researching floating-body memory on bulk silicon, but the 16-nm SOI memory cell they'll present this week—the smallest to date—is made on SOI. Intel's Mayberry says that conventional DRAM will eventually have a scalability problem and that floating-body memory could take over from there. "But as long as you can continue to scale the conventional, it has a leg up," he says. How soon DRAM's demise will come is still up for debate. "The end often gets predicted many times before it gets there," Mayberry adds.

Not everyone is as conservative in their outlook on floating-body memory and SOI. "It's an absolutely dynamite technology," says Bob Merritt, vice president of memory products at Semico Research Corp., a semiconductor marketing research and consulting company.

Merritt thinks the reason it's so dynamite is because there is a shift away from desktop computing and toward memory for mobile devices, along with a growing concern for power consumption. So any technology that will lead to smaller or more-efficient devices will garner significant research.

He thinks that floating-body memory and SOI will first emerge as embedded memory, not DRAM. "In that case, the floating-body SOI technology offers some immediate benefits—lower die size and lower cost," Merritt says. Microprocessor makers—with Intel a notable exception—are also increasingly using SOI wafers with great results in terms of performance and energy consumption, says Merritt.

On the other hand, stand-alone DRAM is already well understood, and aside from future scalability issues, there isn't an immediate reason to push a new, less-understood technology. "It will take more SOI research to use [floating-body memory] as a DRAM-type application," Merritt says.

So if floating-body memory is really all it's cracked up to be, why haven't we seen it yet in a real product? "It usually takes about 10 years for new technology to reach production," Innovative Silicon's Lewis says. And floating-body memory is competing against a well-understood and time-tested technology. "In the past 20 to 30 years, the only new memory technology that's gone to high production is flash," adds Jones. "It's not something the industry does every day of the week."