

Join us at DEVCON.
Be sure and catch *Jamie Hyneman* and *Adam Savage* – at DEVCON 2008.



Register Now!
Oct. 13-15
San Diego

DEVCON
Breaking the Myth
RENESAS | 2008



EE Times: [Semi News](#)

Intel, Chartered slam semi IP industry

[Mark LaPedus](#)

(09/26/2008 12:30 PM EDT)

URL: <http://www.eetimes.com/showArticle.jhtml?articleID=210604186>

SANTA CLARA, Calif. -- For some time, the semiconductor intellectual-property (IP) industry has been the virtual and ongoing punching bag in the IC business.

Lack of standards, quality metrics and business models have hurt the IP industry for years. Profitability remains elusive for many IP vendors. And most--if not--all of those problems continue to haunt the industry as a whole.

At the GSA IP conference here this week, two chip makers--Intel Corp. and Chartered Semiconductor Manufacturing Pte. Ltd.--took turns in separate presentations and landed some pot shots at the semiconductor IP industry for those and other reasons.

"Customers are aggravated and frustrated with the business models," said Walter Ng, vice president of design enablement alliances with Singaporean foundry provider Chartered, during a presentation at the event.

"There is a problem with the third-party IP vendors in terms of scaling," Ng said. And in terms of IP quality standardization, "there is a lot to be done in that area."

Ng did not identify which IP vendors are dragging down the industry, nor did he point the finger at one company.

Clearly, some IP houses are better than others. Deserved or not, the industry as a whole is to blame for the shaky--if not poor--reputation in the large and complex IP sector. In total, there are 300-to-400 semiconductor IP vendors of all shapes and sizes. ARM, Cadence, MIPs, Rambus, Virage and Synopsys are among the bigger players, but most IP vendors are small-sized shops.

Semico Research Corp. projects that the IP market will grow 18 percent through 2012. The IP business is expected to grow faster than the overall semiconductor industry, said Jordan Selburn, an analyst with iSuppli Corp.

But after three years' of double-digit growth rates, the IP market settled back to 8 percent growth during 2007, according to Gartner Inc. "Moreover, as growth rates decline, we believe that small to midsize IP vendors should prepare to acquire other companies, or be acquired, as consolidation has become IP vendors' key strategy for gaining scale and remaining in the market," according to a recent report from Gartner.

Without a doubt, semiconductor IP remains critical for the industry to enable new designs. But after years' of talk and promises, the IP community is still unable to get its act together.

There is a "positive trend" in terms of the evolution of better IP quality, but some vendors still lack good integration practices, said Ken Tallo, director of external IP and virtual platforms at Intel, during a separate presentation at the event.

"Good design practices are not enough" in the IP industry, Tallo said.

The ongoing problem is deciding what IP has been actually validated and integrated in the design flow, he said. And there are several ongoing and nagging issues with IP: common ABIs, verification and behavioral models, he said.

In the IP community, the verification methodologies "are not consistent," Tallo said. Finding predictable system-level behavioral models are "also a challenge."

As a result, chip makers and IP vendors have been calling for standards in the last several years. And the time is still ripe for standards. "It's time for the IP users to align on a common set of integration standards," he said.

IP vendors must also step up to the plate. "There are a lot of IP vendors doing the same thing," Chartered's Ng said. "I see a lot of IP companies that don't take risks."

The solution? At least one solution is that IP vendors must "come out of their silos" and "collaborate" to "become more competitive," he added.

One vendor defended the IP community. "We've made a lot of progress as an industry," said John Chilton, senior vice president of marketing and corporate development at Synopsys Inc.

Adam Traidman, group marketing director at Cadence Design Systems Inc., said the IP vendors themselves are moving towards better and more "flexible business models."

Over time, IP has been easier to integrate and has seen a shift towards higher-quality products, he said. Traidman was the boss of Chip Estimate. Recently, Cadence acquired IP reuse specialist Chip Estimate.

The industry is also making progress in terms of metrics. Last year, for example, the GSA (formerly Fabless Semiconductor Association) announced the release of its IP assessment tool. The product, dubbed the Hard Intellectual Property (IP) Quality Risk Assessment Tool version 3.0, collects information about an IP vendor and its design methodology.

Synopsys' Chilton also pointed towards the TLM-2.0 standard as another key IP effort. The Open SystemC Initiative (OSCI), an independent non-profit organization dedicated to defining and advancing SystemC, recently announced Tallo as the new chairman. SystemC is a language built in C++ that spans from concept to implementation in hardware and software.

In December 2007, OSCI released a second draft of its Transaction-level Modeling Standard (TLM) 2.0 standard. The proposed standard is claimed to assure interoperability between IP models, system models and system-level design tools.

In June, the OSCI announced the completion of TLM-2.0. The TLM interface standard enables SystemC model interoperability and reuse at the transaction level, providing an essential ESL framework for architecture analysis, software development, software performance analysis, and hardware verification.

"TLM-2.0 addresses the real-world interoperability of transaction level models," Tallo said in a recent statement. "It helps streamline the integration of models from different suppliers without compromising their simulation speed, while allowing for continued advances in TLM performance, productivity and usability. OSCI members and SystemC users from around the world have an active role in the standardization process and are now working diligently across the ESL ecosystem to incorporate TLM-2.0."

In a somewhat rival effort, Mentor Graphics Corp. and Cadence this month announced the release of the latest version of the open-source Open Verification Methodology (OVM). OVM 2.0 includes the new OVM User Guide, which provides step-by-step guidelines to help users develop reusable, interoperable verification IP and hierarchical environments to facilitate plug-and-play verification. The Open Verification Methodology, based on IEEE Std. 1800-2005 SystemVerilog standard.

The new release extends the proven sequential stimulus mechanism in the OVM with TLM interfaces to improve the modularity and reuse of stimulus sequences. Other enhancements include direct support for parameterized classes in the OVM factory and built-in debug support for TLM connections throughout the hierarchy.

"The release of version 2.0 of the OVM is a significant event for verification teams," said Tommy Kelly, CEO of Verilab, in a recent statement. "It builds on the previous release of the methodology, further enhances the capabilities of engineers interested in reusable, interoperable verification environments, and strengthens overall the case for using the OVM. Verilab is deploying the OVM in its own verification IP development, and supports the use of the methodology at several of its international clients."

Another group, the Spirit consortium, a non-profit organization developing an XML based metadata standard to allow multiple facets of a circuit block to be defined, in March announced that it was ready to move the standard up from the register transfer level (RTL) to support transactional and mixed modeling styles.

The move from version 1.2 to version 1.4 also involved the definition of an additional interface known as the tight generator interface (TGI).

The IP-XACT specification, an XML databook that documents many different aspects of IP modules, enables designers to create many different expressions of a design automatically and in a consistent way. Spirit officers emphasized at the show that one metadata starting point can benefit both design and verification engineers.

Still another group, the OCP International Partnership Association Inc. (OCP-IP), in May announced the release of OCP 2.2 Revision A. The latest version of the specification now includes several consensus profiles. Consensus profiles provide company engineers with standardized configurations of OCP options for specific system use cases, ensuring interoperability without conversion, increasing productivity and speeding time to market.

The OCP-IP promotes and supports the Open Core Protocol (OCP) as the complete socket standard ensuring rapid creation and integration of interoperable virtual components.

All materials on this site [Copyright © 2008 TechInsights, a Division of United Business Media LLC](#). All rights reserved.

[Privacy Statement](#) | [Your California Privacy Rights](#) | [Terms of Service](#) | [About](#)

You want numbers?

EE|Times

 techonline

Embedded
Systems Design

