

Achronix Semiconductor Ships Field Programmable Gate Arrays (FPGAs)



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Achronix Semiconductor announced that it has started shipping its Field Programmable Gate Arrays (FPGAs). The Speedster family with the SPD60 will be its initial member and is capable of delivering high speeds.

Achronix Semiconductor is a fabless corporation building fast Field Programmable Gate Arrays (FPGAs). These employ a unique picoPIPE acceleration technology which offers up to 1.5 GHz peak performance.

The company's Speedster family of FPGAs is most suitable for applications which need ASIC-like performance like in networking, telecommunications, test and measurement, encryption and other high-performance applications.

Achronix and other synthesis vendors have collaborated to make tools and methodologies which are compatible with the Speedster family. Designers will benefit from their existing Verilog and VHDL designs. Synopsys (formerly Synplicity) Synplify Pro and Mentor Graphics' Precision Synthesis tools for RTL synthesis are supported by the Achronix CAD environment.

The Achronix CAD environment also offers tools required for physical implementation, performance optimization, timing analysis, simulation, debug, and device programming.

"Designers have been lulled into expecting only incremental performance improvements with each new generation of FPGA," said John Holt, Achronix founder, chairman and CEO. "Our product provides a disruptive leap in performance that opens up new worlds of application design previously unavailable to engineers using FPGAs."

The Speedster family of FPGAs utilizes the picoPIPE acceleration technology which can speed up the data flow through the FPGA fabric. As there is no global clock, picoPIPE uses simple handshake protocols for controlling data flow. This improves performance greatly using standard RTL for design-entry and using FPGA tools.

Rich Wawrzyniak, senior market analyst at Semico Research Corp. said that the FPGA market needs an innovative approach. Achronix combines the benefits of their picoPIPE technology with a synchronous interface, coupled with an experienced team of FPGA industry executives and designers to provide an FPGA with ASIC-like performance.

This innovative technology can be used with a 10.3 Gbps serializer/ deserializer (SerDes) for providing high system throughput and integrated DDR2/DDR3 controllers for a fast memory interface. The Speedster family also provides the I/O speed required to match the core performance. The process used to manufacture the device is the TSMC's high performance 65 nm G+ CMOS process.

Speedster FPGAs include a new DDR2/DDR3 solution which includes a physical layer and controller supporting memory interface speeds of 1066 Mbps. The picoPIPE technology is tolerant to wide variations in supply Voltage enabling users with a power-management tool.

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