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## Achronix Semiconductor Launched to Break through FPGA Performance Barriers

**-- Company leverages patented picoPIPE(TM) acceleration technology to deliver the world's fastest FPGA, capable of 1.5 GHz peak performance. -- First device in the Speedster(TM) family embeds 20 lanes of 10.3 Gbps SerDes and four independent 1066 Mbps DDR2/DDR3 controllers. -- Speedster uses familiar LUT-based fabric and standard synthesis and simulation tools so designers can use their existing RTL.**

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SAN JOSE, Calif., Sep 16, 2008 (BUSINESS WIRE) -- Signaling a breakthrough in three decades of field-programmable gate array (FPGA) design where performance has been sacrificed for flexibility and time-to-market, Achronix Semiconductor today announced that it has already begun shipping the world's fastest FPGAs. The Speedster family, with the SPD60 as its initial member, delivers speeds up to 1.5 GHz, which represents a three-fold increase in performance over existing FPGAs.

Achronix early engagement customers have already found success with Speedster in applications requiring ASIC-like performance namely networking, telecommunications, test and measurement, encryption and other high-performance applications. These types of applications are an ideal fit for the Speedster family of FPGAs.

Achronix has partnered with leading synthesis vendors to make industry-standard tools and methodologies compatible with the Speedster family. Designers can leverage their existing Verilog and VHDL designs. The Achronix CAD environment supports both Synopsys (formerly Synplicity) Synplify Pro and Mentor Graphics' Precision Synthesis tools for RTL synthesis. In addition, the Achronix CAD environment provides the necessary tools for physical implementation, performance optimization, timing analysis, simulation, debug, and device programming.

"Designers have been lulled into expecting only incremental performance improvements with each new generation of FPGA," said John Holt, Achronix founder, chairman and CEO. "Our product provides a disruptive leap in performance that opens up new worlds of application design previously unavailable to engineers using FPGAs."

The Speedster family of FPGAs uses the Achronix patented picoPIPE acceleration technology that speeds the way data moves through the FPGA fabric. In the absence of a global clock, picoPIPEs use simple handshake protocols to efficiently control data flow, resulting in significantly improved performance, all along using standard RTL for design-entry and employing familiar FPGA tools. By coupling this innovative technology with a 10.3 Gbps serializer/deserializer (SerDes) to facilitate high system throughput and integrated DDR2/DDR3 controllers for high-speed memory interface, the Speedster family provides the I/O speed to match its outstanding core performance. The device is manufactured in TSMC's high performance 65 nm G+ CMOS process.

"The FPGA market is a tough arena to enter and a truly innovative approach is needed to compete and succeed in this space," said Rich Wawrzyniak, senior market analyst at Semico Research Corp. "Based on their innovative approach to combining the benefits of their picoPIPE technology with a synchronous interface, coupled with an experienced team of FPGA industry executives and designers, Achronix appears to be the company that can finally provide an FPGA with ASIC-like performance and deliver a product that can compete with ASIC's at the high end of the market."

More information about the Speedster family

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The Speedster 10.3 Gbps SerDes supports numerous high-speed interfaces, such as 40G/100G Ethernet, CEI-6G, 10 Gbps backplane, XFI, PCI Express (Generations 1 and 2), XAUI, Serial Rapid IO and Infiniband. Speedster FPGAs also includes a complete out-of-the-box DDR2/DDR3 solution which includes a physical layer and controller supporting memory interface speeds of up to 1066 Mbps. A key feature of Achronix' picoPIPE technology is its tolerance to substantial variations in supply Voltage. This gives users a valuable power-management tool. Power consumption can be lowered by adjusting core supply Voltage. Volume pricing for the Speedster FPGA family ranges from under \$200 to \$2500.

#### About Achronix's Management Team and Funding

Achronix's management team consists of key industry veterans who each bring decades of FPGA, ASIC, and structured ASIC design and marketing expertise from several industry stalwarts such as Xilinx, LSI Logic, and Actel. John Lofton Holt -- Achronix's founder, chairman and CEO -- is an experienced entrepreneur and electrical engineer. He leads a team that includes Dr. Rajit Manohar, founder and CTO, who is an internationally recognized pioneer in asynchronous semiconductor design and implementation. New Science Ventures, Battery Ventures, Entrepia Ventures, and Easton Capital Investment Group have invested \$34.4 million in the company to date.

#### About Achronix Semiconductor

Achronix Semiconductor is a privately held fabless corporation based in San Jose, California. Achronix builds the world's fastest field programmable gate arrays (FPGAs) which use a unique patented picoPIPE(TM) acceleration technology capable of up to 1.5 GHz peak performance. Achronix also has sales offices and representatives in the US, Europe, China, Japan, and Korea, and has research and design offices in Ithaca New York and Bangalore India. Find out more at <http://www.achronix.com>.

SOURCE: Achronix Semiconductor

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