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FPGAs are all set for next process nodes

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[Altera](#) Corp. is the first [FPGA](#) vendor to launch a family of 40nm FPGAs. Its rival, [Xilinx](#) Inc., is reportedly pushing for a 45nm line. However, Xilinx still has to announce product updates.

In addition to the Stratix IV FPGAs, Altera will announce 40nm HardCopy IV structured ASICs, as well as corresponding software tools for both device types. Fabricated in Taiwan Semiconductor Manufacturing Co. Ltd's 40nm foundry process, the families promise to enable a new class of single-chip, multicore and related complex devices.

The company had been talking in general terms about 40nm FPGAs for some time.

Unlike Altera, Xilinx has been reluctant to discuss its next-node plans and has insisted that 65nm FPGAs will be the mainstream technology to come. Other FPGA houses are believed to be far behind both companies on the process-technology curve.

Altera is not the first vendor to announce a 40nm [ASIC](#). IBM Corp. rolled a standard-cell ASIC line based on 45nm and silicon-on-insulator technologies. However, Altera was the first vendor to release information on a 40nm structured ASIC.

The previous shift to 40nm gives the company "a strong competitive lead," said John Daane, president, CEO and chairman of Altera. Daane dropped hints about the 40nm FPGA line, but did not elaborate product details. He called Altera the "lead customer" for TSMC's 40nm process, which debuted in March.

Altera is expected to ship the first of its 40nm FPGAs by the end of 2008. Judging by the process schedules of rival foundries, Xilinx might not be far behind. One of its two foundry partners, United Microelectronics Corp., is set to ship its initial 45nm/40nm wafers by the end of the year. Xilinx's other foundry partner, Toshiba Corp., claimed to be in 45nm logic production.

"I assume you will see a 45nm/40nm product from Xilinx that will be out soon," said Rich Wawrzyniak, analyst at Semico Research Corp. He added these are the early days for the market and predicted the next-node devices will represent only 1, 2 or 3 percent of the total FPGA volumes this year.

"Altera's new FPGAs and ASICs are pretty impressive, but I'm sure the parts won't be cheap," Wawrzyniak noted.

Chuck Tralka, senior director of product marketing at Xilinx, said Altera's pushing to 40nm FPGAs is an effort to "shift the attention away from the 65nm FPGA market, where it has not been successful." Xilinx claimed to have a 2:1 edge in market share over Altera in high-end FPGAs at the 65nm node.

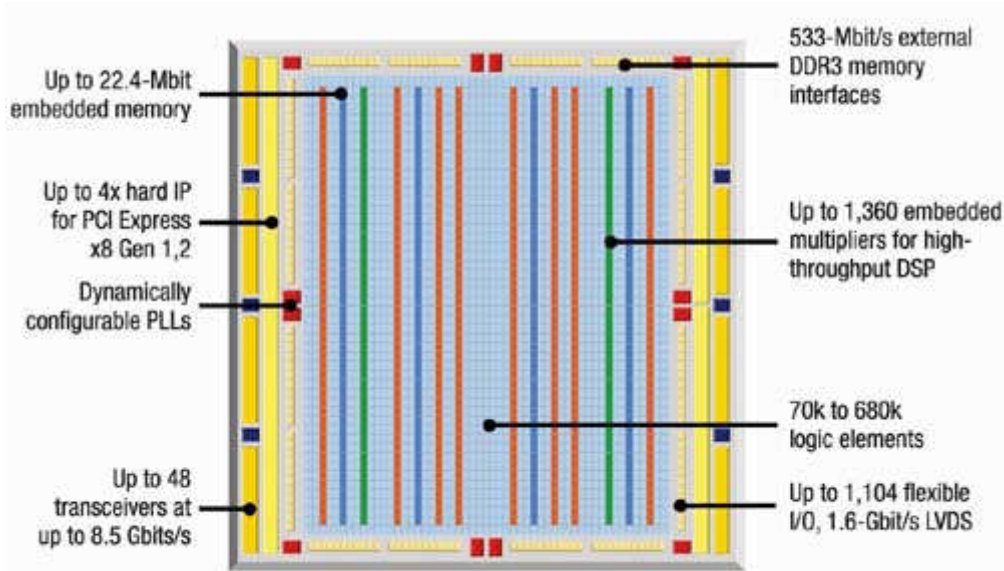
Tralka said 90nm FPGAs remain "a significant revenue generator," but added that, "the bulk of the design activity is targeted at 65nm."

Not surprisingly, Altera reacted to Xilinx's assertions. In Q1 08, Daane said, "Altera saw a 198 percent jump in shipments for the Stratix III, its high-end 65nm FPGA line."

"Altera will continue to sell the Stratix III for some time, but our customers have asked us to be more aggressive in process technology," said David Greenfield, senior director of product marketing for high-end FPGAs.

Complementary mix

Altera offers PLDs as well as ASICs and FPGAs, viewing the categories as complementary. "Designers can use the company's HardCopy methodology to develop a prototype on an FPGA, then move into production with a structured ASIC," Greenfield added, noting that the 40nm technology will enable a new class of system-level products.



Source: Altera

Altera's 40nm FPGA wonder: The company claims highest-density device with Stratix IV.

"It's not hard to imagine that you could put a couple of hundred cores on the same FPGA device at 40nm," said Wawrzyniak. "I don't think people will do that, but I would not be surprised to see 8 or 16 cores within an FPGA," he added.

The devices include 12 entries in the Stratix IV FPGA line and 12 in the HardCopy IV structured-ASIC family. The Stratix IV is believed to have twice the density of the company's 65nm Stratix III. One Stratix IV entry supports up to 48 transceivers operating at up to 8.5Gbit/s.

The Stratix IV FPGAs have a core performance of 350MHz, identical to that of the Stratix III devices, but add new hard IP blocks to enhance performance. Both the 65nm and 40nm families contain DSP and memory blocks that run in excess of 550MHz, as well as [PCIe](#) hard IP blocks running at 500MHz. "Like the 65nm versions, the Stratix IV devices feature Altera's Programmable Power Technology, which optimizes logic, DSP and memory blocks to help manage static power," Greenfield said.

The Stratix IV comprises two lines: an enhanced memory/DSP offering (Stratix IV E); and a variant with transceivers (Stratix IV GX). The top entry in the GX line has 530,000 logic elements, 48 transceivers, 20.3Mbits of memory and 1,024 18 x 18 multipliers. The high-end E entry has 680,000 logic elements, 22.4Mbits of memory and 1,360 18 x 18 multipliers.

The HardCopy IV ASIC family offers equivalent densities to the Stratix IV devices and features up to 13.3 million gates. For the first time, Altera is offering a transceiver-based ASIC option with HardCopy IV.

Altera said the new Quartus II software v.8.0 delivers, on average, three times the compile speed for high-end FPGAs compared with the nearest competitor's latest offering.

Engineering samples of the first Stratix IV entry are slated for the Q4. Customer tapeouts for HardCopy IV ASICs will start in the Q3 09.

- Mark LaPedus

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