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## Virage Logic Delivers Open RTL to Test Floor Embedded Memory Test and Repair Subsystem

*New Release of STAR Memory System Expands Availability of Subsystem Beyond Virage Logic Memories to Third-Party and Internally Developed Memories*

FREMONT, Calif.--([BUSINESS WIRE](#))--Virage Logic Corporation (NASDAQ: VIRL), the semiconductor industry's trusted IP partner and pioneer in Silicon Aware IP™, today announced the availability of a completely open register transfer level (RTL) to test floor embedded memory test and repair subsystem based on the latest release of its flagship Self-Test and Repair (STAR™) Memory System and the recently introduced STAR™ Yield Accelerator. The new release of the STAR Memory System features an open memory interface, giving System-on-Chip (SoC) designers the freedom to use the system's capabilities with their choice of Virage Logic memories, other commercially available third-party memories or internally developed embedded memories.

The STAR Memory System, when used in conjunction with the STAR™ Yield Accelerator, provides a complete RTL to test floor embedded memory test and repair solution that addresses the needs of SoC designers, test and product engineers. Created to reduce time-to-tapeout and accelerate time-to-volume, the STAR Yield Accelerator bridges the design and manufacturing disciplines to enable automated test vector generation, silicon debug, fault isolation and classification to be used at the critical semiconductor characterization, bring-up, volume manufacturing and electrical failure analysis stages.

"Virage Logic is unique in that it is the only company that has expertise in both memory design and memory silicon analysis," noted Richard Wawrzyniak, senior market analyst, ASIC and SoC for Semico Research. "This expertise provides the basis for Virage Logic to deliver a complete RTL to test floor embedded memory test and repair subsystem, which is critical in helping semiconductor companies quickly ramp to volume, particularly at the advanced process technologies of 65 and 40-nanometer. And, by opening up the STAR Memory System, Virage Logic is able to provide its highly sophisticated embedded test and repair technology to the masses."

"Virage Logic has long been recognized as the industry expert in providing superior test and repair solutions that enable designers to quickly and efficiently ramp their designs to volume manufacturing at advanced nodes," said Dr. Yervant Zorian, Virage Logic's vice president and chief scientist. "The new release of the STAR Memory System features enhanced fault-detection capabilities to identify new defects emerging at advanced process nodes. As such, the system tracks an expanded set of faults, including challenging resistive, transition, and dynamic faults to meet today's test escape level goals. In addition, the new release of the STAR Memory System includes hierarchical insertion and verification of a test and repair subsystem, as well as structures for low power design, to address the dramatic increase in design complexity."

"By providing a new open interface to the STAR Memory System, we extend the value of the system to users regardless of whether they elect to use Virage Logic memories, other commercially available or internally developed memories," said Brani Buric, vice president of product marketing and strategic foundry relationships. "Users can leverage the flexibility of being able to mix memories from various sources to meet their specific design requirements and still utilize the most advanced test and repair solution, contributing to greater design flexibility and higher quality end products."

## **About Virage Logic's RTL to Test Floor Embedded Memory Test and Repair Subsystem**

The STAR Memory System provides the most integrated cost-effective solution for embedding on-chip test and repair of memories in designs with a few to a few-thousand memory instances. Repairable or non-repairable embedded memories across any foundry or process node can be incorporated as part of the STAR Memory System to address a broad range of SoC design requirements. The STAR Memory System consists of a complete solution allowing users to select and automatically integrate and verify all of the components required within the system. The STAR™ Shared Fuse Processor allows users to reduce routing complexity and drastically reduce fuse area, while the STAR™ Builder automated integration tool enables users to better meet aggressive time-to-volume requirements. Already silicon proven in hundreds of designs on a variety of process nodes ranging from 180nm to 55nm, the STAR Memory System provides the most complete test solution to improve test quality, repair of manufacturing faults found in advanced processes and ease of integration into design.

In order to provide STAR Memory System access to all memory developers, Virage Logic has developed a proprietary memory description language called MASIS. The MASIS language, together with a MASIS compiler, simplifies and accelerates the process of creating and verifying memory views used by the STAR Memory System.

The test floor component of Virage Logic's complete solution, STAR Yield Accelerator, addresses the requirement to rapidly, cost-effectively and accurately identify, analyze, isolate and classify memory faults as designs are readied for transition from first silicon to volume manufacturing. The STAR Yield Accelerator consists of the STAR Verifier, STAR Vector Generator and STAR Debugger components. Leveraging the infrastructure of the STAR Memory System, the STAR Yield Accelerator automatically generates vectors for test equipment and provides fault analysis and root-cause failure guidance based on silicon test results. Using STAR Yield Accelerator, test and product engineers can rapidly analyze failures manifested in embedded memories and inspect the physical location and class of each fault to determine the root cause without involving the IP vendor or SoC designer.

Working in concert to provide a complete RTL to test floor embedded memory test and repair solution, the STAR Memory System is proven to reduce tapeout schedules for new complex SoCs by weeks and the STAR Yield Accelerator can reduce silicon bring-up by months, reducing overall time-to-volume production.

### **Pricing and Availability**

The newest release of Virage Logic's STAR Memory System, supporting Virage Logic, third-party and internally developed memories, is now available and can be licensed on a project basis with pricing starting at \$25,000. STAR Yield Accelerator is also available today. Project-based engagements include software and services with pricing starting at \$50,000.

### **About Virage Logic**

Founded in 1996, Virage Logic Corporation rapidly established itself as a technology and market leader in providing advanced embedded memory intellectual property (IP) for the design of complex integrated circuits. The company's Silicon Aware IP™ offering (embedded memories, logic libraries and I/Os) includes silicon behavior knowledge for increased predictability and manufacturability. Through its acquisition of Ingot Systems in 2007, the company expanded its product offering to include Application Specific IP (ASIP) solutions such as Double Data Rate (DDR) Memory Controllers and design services. The highly differentiated product portfolio provides higher performance, lower power, higher density and optimal yield to foundries, integrated device manufacturers (IDMs) and fabless customers. The company uses its FirstPass-Silicon Characterization Lab™ for certain products to help ensure high-quality, reliable IP across a wide range of foundries and process technologies. For more information, visit [www.viragelogic.com](http://www.viragelogic.com).

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