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Altera 40-nm lineup pushes FPGAs to next process node

[Mark LaPedus](#)

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Editor's Note: Meet the designers behind Altera's 40-nm chip and hear more about the hurdles they overcame by clicking [video](#). For expert analysis, click [here](#).

Altera Corp. today is expected to become the first field-programmable gate array vendor to announce a family of 40-nanometer FPGAs. Rival Xilinx Inc. is reportedly readying a 45-nm line but has yet to announce product.

In addition to the Stratix IV FPGAs, Altera will announce the 40-nm HardCopy IV structured ASICs, as well as corresponding software tools for both device types. Fabricated in Taiwan Semiconductor Manufacturing Co. Ltd.'s 40-nm foundry process, the families promise to enable a new class of single-chip, multicore and related complex devices.

Altera has been talking in general terms about 40-nm FPGAs for some time, though a source at Xilinx speculated Altera has been pumping up the 40-nm development to deflect attention from the lackluster market for its 65-nm lineup.

Unlike Altera, Xilinx has been reluctant to discuss its next-node plans and has insisted that 65-nm FPGAs will be the mainstream technology for some time to come. Other FPGA houses are believed to be far behind both companies on the process-technology curve.

Altera is not the first vendor to have announced a 40-nm ASIC. Last year, IBM Corp. rolled a standard-cell [ASIC](#) line based on 45-nm and silicon-on-insulator technologies. But Altera is the first vendor to release information on a 40-nm structured ASIC.

The early shift to 40 nm gives Altera "a strong competitive lead," John Daane, president, CEO and chairman of Altera, said during a conference call with analysts. Daane dropped hints about the 40-nm FPGA line during the call but did not provide product details, though he called Altera the "lead customer" for TSMC's 40-nm process, which debuted in March.

Altera is expected to ship the first of its 40-nm FPGAs by the end of the year. Judging by the process schedules of rival foundries, Xilinx might not be far behind: One of its two foundry partners, United Microelectronics Corp. (UMC), is expected to ship its initial 45-/40-nm wafers by year's end. Xilinx's other foundry partner, Toshiba Corp., claims to be in 45-nm logic production.

"I assume you will see a [45-/40-nm] product from Xilinx that will come out soon," said Rich Wawrzyniak, an analyst with Semico Research Corp. (Phoenix). But he added that it's early days for the market and predicted the next-node devices will represent only "1, 2 or 3 percent of total [FPGA] volumes" this year.

Altera's new FPGAs and ASICs are "pretty impressive," Wawrzyniak added, but "I'm sure the parts won't be cheap."

Chuck Tralka, senior director of product marketing for Xilinx (San Jose), said Altera's rush to 40-nm FPGAs is an effort to "shift the attention away from the 65-nm FPGA market, where [Altera] has not been successful." Xilinx claims to have a 2:1 edge in market share over Altera in high-end FPGAs at the 65-nm node.

Tralka said 90-nm FPGAs remain "a significant revenue generator" but added that "the bulk of the design activity is targeted at 65 nm."

Not surprisingly, Altera took issue with Xilinx's assertions. In the first quarter of 2008, Daane said, Altera saw a 198 percent jump in shipments for its high-end 65-nm FPGA line, the Stratix III.

Altera will continue to sell the Stratix III for some time, but "our customers have asked us to be more aggressive in process technology," said David Greenfield, senior director of product marketing for high-end FPGAs.

Altera offers PLDs as well as ASICs and FPGAs, viewing the categories as complementary. Designers can use Altera's HardCopy methodology to develop a prototype on an FPGA, then move into production with a structured ASIC. Greenfield said the 40-nm technology will enable a new class of system-level products.

"It's not hard to imagine that you could put a couple of hundred cores on the same [FPGA] device" at 40 nm, said Semico's Wawrzyniak. "I don't think people will do that, but I would not be surprised to see 8 or 16 cores" within an FPGA.

The devices to be announced today include 12 entries in the Stratix IV FPGA line and 12 in the HardCopy IV structured-ASIC family. The Stratix IV is said to have twice the density of the company's 65-nm Stratix III. One Stratix IV entry supports up to 48 transceivers operating at up to 8.5-Gbits/second.

The Stratix IV FPGAs have a core performance of 350 MHz, identical to that of the Stratix III devices, but add new hard IP blocks to enhance performance. Both the 65- and 40-nm families contain DSP and memory blocks that run in excess of 550 MHz, as well as [PCI Express](#) hard [IP](#) blocks running at 500 MHz. Like the 65-nm versions, the Stratix IV devices feature Altera's Programmable Power Technology, which optimizes logic, DSP and memory blocks to help manage static power, Greenfield said.

The Stratix IV comprises two lines: an enhanced memory/DSP offering (Stratix IV E) and a variant with transceivers (Stratix IV GX). The top entry in the GX line has 530,000 logic elements, 48 transceivers, 20.3 Mbits of memory and 1,024 18 x 18 multipliers. The high-end E entry has 680,000 logic elements, 22.4 Mbits of memory and 1,360 18 x 18 multipliers.

The HardCopy IV ASIC family offers equivalent densities to the Stratix IV devices and features up to 13.3 million gates. For the first time, Altera is offering a transceiver-based ASIC option with HardCopy IV.

The new Quartus II software v.8.0 delivers, on average, three times the compile speed for high-end FPGAs compared with the nearest competitor's latest offering, according to Altera.

Engineering samples of the first Stratix IV entry are slated for the fourth quarter. Customer tapeouts for HardCopy IV ASICs will start in the third quarter of 2009.

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