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Reuse methodology makes more of IP assets

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Semiconductor designers can now license a proven IP core reuse methodology and toolset from IPextreme

NXP Semiconductors' internally developed CoReUse methodology and QCore tool are now available for licensing through IPextreme. CoReUse represents more than ten years of investment by NXP to develop a comprehensive, practical, and efficient system that can be deployed at the group and enterprise level for engineers to develop reusable, high quality IP.

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Clock generator IP offers more than PLLs

Patented digital clock synthesis technology developed by Motorola is now offered to the global semiconductor market through IPextreme

IP core puts 1394b Link Layer on FPGA

The increased bandwidth of the 800Mbit/s 1394b bus will accelerate applications such as storage systems, digital cameras, printers and other computer peripherals

It is in use today by nearly every NXP design group worldwide as the standard by which IP is developed and shared across the company.

CoReUse consists of a series of specifications, guidelines, and templates that guide engineers in developing reusable digital, analogue mixed signal (AMS), and RF IP and includes the CoReUse Foundation, a set of reference manuals that include the CoReUse standard and constraints that define directory structures, naming conventions, and quick reference cards for Verilog and VHDL designs.

Other components include: design for test (DfT) specifications for CTAG/IEEE1500, and support for testing AMS and high-speed IO technologies; an additional set of specifications targeted for AMS and RF IP; system level specifications for transaction level modelling, SoC integration using SPIRIT IP-Xact and PSL assertions; architectural level specifications for using on-chip buses allowing the creation of IP-based platforms; and documentation templates for engineers to capture key information about the IP they are developing.

An important companion to the CoReUse standard is QCore, an EDA tool internally developed by NXP to automatically check an IP's deliverables and documentation for compliance to the standard.

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QCore produces a certificate that classifies IP according to its compliance level to the CoReUse standard allowing integrators to know the level of completeness and quality achieved by that IP.

Further reading

Memory compilers streamline SoC design

The SiWare Memory compilers and SiWare Logic libraries provide designers with options for maximum flexibility in effectively managing design tradeoffs to meet their specific requirements

PCI Express endpoint controller runs on FPGAs

The DesignWare LE IP for PCIe is a cost-effective solution that provides innovative ease-of-use features to simplify the complexities of transitioning to PCI Express

Multiprocessor core incorporates multithreading

The 1004K core optimises CPU performance on a shared memory system, enabling multiple functions and applications to be implemented in a single product



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NXP has long been a thought leader in driving higher productivity in the [semiconductor industry](#) by pioneering advances in IP-based design and is an active participant in industry-wide IP standardisation initiatives.

Ralph von Vignau, Senior Director in NXP's Corporate Innovation and Technology group and President of the SPIRIT Consortium, comments: 'NXP sees how opening up CoReUse for broad adoption can lead to faster progress on standardisations needed in the IP industry, allowing companies to more efficiently develop and share IP internally and between companies'.

Industry initiatives like VSIA have highlighted the difficulty the industry has experienced in creating, executing, and maintaining a standard IP reuse methodology.

'CoReUse represents a giant step forward in what's available for a company to develop high quality reusable IP', says Warren Savage, President and CEO of IPextreme.

'CoReUse and QCore, provide something for everyone'.

'For engineers it's a means to do your job better; for managers, it's a tool for getting the maximum output and quality out of your teams; and for executives, it's a technology that enables engineers and managers to make your organisation as efficient and profitable as possible'.

'By making the CoReUse methodology widely accessible, we are giving the design community a proven and valuable methodology and tool set that they can unwrap and use productively straight out of the box'.

'NXP has made an astute analysis of IP trends', says Richard Wawrzyniak, Senior Market Analyst, ASIC and SoC, Semico Research Corp.

'IP reuse is going to continue to increase'.

'It's just a matter of time before everyone in the design flow has to pay more attention to reuse, and an established design reuse methodology should help the whole industry'.

CoReUse and QCore are available today.

Customers can purchase the CoReUse standard in the form of e-books for as low as US \$199 per user per year from IPextreme's Core Store.

Training for CoReUse is offered to companies who desire more in-depth instruction on its effective use.

QCore is offered on a per-seat licence basis as well as enterprise-wide licences.

Customisation services are also offered for those companies wanting to blend their own best practices with what's available in CoReUse.

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