Virage Logic First to Deliver Complete Memory Compiler and Logic Library IP Portfolio for TSMC 40nm Process

2008-04-07 13:18:48 -

www.viragelogic.com - Virage Logic Corporation Sabina Burns, 510-743-8115 sabina.burns@viragelogic.com or McClenahan Bruer Communications James McIntyre, 503-546-1000 james@mcbru.com Virage Logic Corporation (NASDAQ:VIRL), the semiconductor industry's trusted IP partner and pioneer in Silicon Aware IP (TM), today announced the availability of memory compilers and logic libraries for TSMC's 40-nanometer (nm) process. The new SiWare(TM) product portfolio provides semiconductor companies with 40nm physical IP that is designed to enable System-on-Chips (SoCs) to run faster, manage power more efficiently, use less area, and achieve higher manufacturing yields.

The SiWare product line, first introduced in October 2007 for the 65nm process, addresses the increasingly complex design requirements placed on physical IP at advanced process nodes. The SiWare Memory compilers and SiWare Logic libraries provide designers with a complete "dashboard" of options for maximum flexibility in effectively managing design tradeoffs to meet their specific requirements.

As the first commercial IP provider with memory compiler and logic library IP in use on TSMC's 40nm process, Virage Logic offers customers early access to design more competitive chips at reduced risk while helping enable them to take advantage of significant cost savings. Primary end markets for SiWare IP on TSMC's 40G process include computer, graphics, networking and storage applications, while primary end markets for SiWare IP on TSMC's 40LP process include wireless, battery-operated and consumer applications. With its advanced tradeoff capabilities, SiWare Memory users can achieve static power savings of up to 35 percent, 70 percent and 90 percent depending on their selection of the built-in light sleep, deep sleep and shut-down modes available in both the 40G and 40LP memories.

Building on the tradeoff capabilities introduced in the 65nm SiWare product line to enable optimal management of performance, area, power and statistical yield, the 40nm SiWare offering includes advanced built-in power management capabilities that will enable designers to mitigate high power consumption at this advanced process node.

"With the SiWare 40nm announcement, our customers can benefit by taking advantage of Virage Logic's IP products to help differentiate their semiconductor products from competitive offerings with respect to speed, area, power management, standby power and yield," said Brani Buric, vice president of product marketing and strategic foundry relationships at Virage Logic. "Virage Logic's broad IP portfolio and extensive silicon validation program enables our customers to reduce design risk, shorten time-to-market and time-to-volume, and lower their development costs. Virage Logic IP provides an exceptional value for customers by offering complete product and service packages -- from small and large projects, to serving as a full, corporate-wide IP partner."

"Virage Logic has a long track record of being first to deliver quality, silicon proven products on each new node," said Rich Wawrzyniak, senior analyst at Semico Research. "The company's new 40nm SiWare offering shows attention to detail in terms of providing a built-in power management solution for SoC designers. With the ability to manage and optimize speed, power, area, and yield tradeoffs, the robust SiWare products enable designers to successfully address the complex challenges of 40nm design. Virage Logic's technology leadership position should provide customers a solid future in investing at 40nm."

About SiWare Memory Compilers and SiWare Logic Libraries

The SiWare Memory product line of silicon aware compilers provides power-optimized memories for advanced processes. These high-performance memory compilers minimize both static and dynamic power consumption and provide optimal yields. SiWare High-Density memory compilers are optimized to generate memories with the absolute minimum area. SiWare High-Speed memory compilers are designed to help designers achieve the most aggressive critical path requirements. Compile-time options for process threshold variants, power saving modes, read and write margin extensions, ultra-low voltage operation, and innovative design for at-speed test enable SoC designers to configure optimal solutions for their specific design requirements. All SiWare memories are fully supported by Virage Logic's STAR(TM) Memory System, the company's flagship integrated embedded memory test and repair system. For repair purposes, the STAR Memory System deploys foundry-developed eFuse for repair signature storage. The STAR Memory System employs test algorithms tailored for advanced processes for higher product reliability and accelerated time-to-yield.

The SiWare Logic product line includes yield-optimized standard cells for a wide variety of design applications at 40nm with multiple threshold process variants. SiWare Logic libraries are offered using three separate architectures to optimize circuits for Ultra-High-Density, High-Speed, or general use. SiWare Ultra-Low-Power extension libraries provide designers with the most advanced power management capabilities.

Availability and Pricing

SiWare Memory compilers and SiWare Logic libraries are available now for early adopters of TSMC's 40G and 40LP processes. Early partners already have internally qualified SiWare IP in silicon. Virage Logic's qualification process, based on advanced test chip methodologies, is in progress and will be finalized as early as July 2008. Project pricing starts at $100,000. The SiWare product portfolio supports all major electronic design automation (EDA) tool flows targeted for the 40nm process including Cadence Design Systems, Magma Design Automation and Synopsys.

About Virage Logic

Founded in 1996, Virage Logic Corporation (NASDAQ:VIRL) rapidly established itself as a technology and market leader in providing advanced embedded memory intellectual property (IP) for the design of complex integrated circuits. Today, as the semiconductor industry's trusted IP partner, the company's Silicon Aware IP offering (embedded memories, logic libraries and I/Os) includes silicon behavior knowledge for increased predictability and manufacturability. Through its recent acquisition of Ingot Systems, the company has expanded its product offering to include Application Specific IP (ASIP) solutions such as Double Data Rate (DDR) Memory Controllers and design services. Virage Logic's highly differentiated product portfolio provides higher performance, lower power, higher density and optimal yield to foundries, integrated device manufacturers (IDMs) and fabless customers who develop products for the consumer, communications and networking, hand-held and portable, computer and graphics, automotive, and defense markets. The company uses its FirstPass-Silicon Characterization Lab(TM) for certain products to help ensure high quality, reliable IP across a wide range of foundries and process technologies. The company also prides itself on providing superior customer support and was named the 2006 Customer Service Leader of the Year in the Semiconductor IP Market by Frost & Sullivan. Headquartered in Fremont, California, Virage Logic has R&D, sales and support offices worldwide. For more information, visit www.viragelogic.com.

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