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EDA and IP

Warren Savage On: The Next Big Thing

by **Warren Savage**

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About 20 years ago, we saw the emergence of the **EDA** industry together with the rise of the independent fabs herald a new era of unprecedented design productivity. Internal CAD groups were systematically dismantled in favour of buying third-party tools, spilling legions of CAD engineers onto the street who formed new EDA companies. And for about 10 years, all was right with the world.

Then about 10 years ago, the EDA industry started to groan under the burden of keeping up with the design productivity demanded by Moore's law. As EDA's answer, we saw the introduction of new technologies in the area of behavioural synthesis and new system level design tools that were aimed at raising the level of design abstraction. The world more or less yawned.

Around the same time, a crop of fresh-faced kids showed up as IP companies. Neither a part of the powerful EDA oligarchy nor the old-money semiconductor industry, companies like ARM and Artisan established their place in a new semiconductor ecosystem by providing pre-designed reusable blocks of IP as the answer for the industry's design productivity demands. The rest is history, as the IP industry has grown at an annual rate of 15-20% for 10 years and continues to outpace the sleepy growth of both semiconductor and EDA. **Semico** predicts that **IP will reach \$5.5B by 2012**, which puts it in striking distance of eclipsing EDA (click on chart below).

So how can that be? What is driving this growth? The answer is simple: Moore's law, which like Einstein's $E=MC^2$, shows no sign of relinquishing its position as "the law". The total amount of gates on a chip keeps going up, while the number of design-starts are holding steady (another **chart** based on data from **iSuppli** shows this effect).

The importance of these trends and ability to participate in the high growth IP market have caused EDA companies to find ways to participate outside their normal tools businesses.

Synopsys, long a player in the IP market with its DesignWare product, has continued to double-down its bets on IP by snapping up companies with standards-based IP for the consumer space and using that IP product line to get closer to design groups.

Cadence has picked up an IP tools and catalogue company, Chip Estimate, as a way of participating in the entire IP ecosystem without actually being in the IP business.

Magma is getting into the IP game with the acquisition of Sabio, which has tools for companies to move physical IP from one process node to another, perhaps signifying a sense that IP companies may represent a reasonable size customer base to serve.

Taking a detour is Mentor Graphics which has recently announced its shuttering of the IP division that develops IP in some of the same markets as Synopsys.

The centrality of IP to semiconductor industry today was perhaps best driven home to me during the IPextreme World 2007 conference in Taiwan last December. In my keynote, I noted that 60% of the silicon area of chips produced today comes from licensed IP. Following me was K.C. Shieh, founder, vice chairman and CEO of **Global Unichip** who quickly informed the audience that "I'm sorry but Warren is wrong, 80% of the area of chips produced by my company come from licensed IP." I hate it when I'm wrong.

Warren Savage, President and CEO of IPextreme, is a well-known and published authority in the field of semiconductor intellectual property. He has a long history of pushing the envelope of design methodology from his work in fault tolerant computing at Tandem Computers in the 1980's and driving reliable design methodologies into commercial practice at Synopsys for its DesignWare IP product in the 1990s.

Much of his thinking became embodied in the seminal book on IP reuse, the Reuse Methodology Manual. Warren is taking his vision to the next level with his latest company, IPextreme, which is focused on enabling broad commercialisation of IP captive in large semiconductor companies.

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