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Virage Logic leverages 65-nm design successes

[Nicolas Mokhoff](#)

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MANHASSET, N.Y. -- Virage Logic is expanding its 65-nm [IP](#) products, with an eye towards tackling today's complex IC-design challenges. The products are based on more than two years of early 65-nm silicon successes.

Virage Logic pioneered a new class of semiconductor IP, called Silicon Aware IP, two years ago. It includes silicon-behavior knowledge for better predictability and manufacturability of leading-edge ICs.

"Because Silicon Aware IP understands the behavior of silicon and is able to address post-silicon issues, it is key in helping designers maximize yield, lower test costs, increase reliability, speed time-to-volume and improve overall manufacturability," said Yervant Zorian, Virage Logic vice president and chief Scientist.

Virage Logic was the first intellectual-property company to tape out a 65-nm test chip, in December 2004. According to Zorian, an important criterion for 65-nm designers is to *really* find a tradeoff among speed, power, area, and yield to find the "sweet spot" for each design.

At the [International Test Conference](#) this week (Santa Clara, Calif.), the company is announcing the availability of a broad new family of 65-nm IP products. The SiWare Memory product line is said to provide a [dashboard](#) that enables SoC designers to explore those tradeoffs to generate optimal [memory](#) configurations. This "dashboard control" capability is critical at 65-nm, where both design and process complexities require sophisticated management of the various tradeoffs in order to effectively meet stringent end-product requirements and increasingly narrow market windows, according to Zorian.

The complementary SiWare Logic product line offers SoC designers that same ability to manage tradeoffs between area, speed and power in logic ICs.

"Since the introduction of our 65-nm offering with TSMC, UMC and Freescale in 2004, we have leveraged our early experience to provide designers with an advanced product offering that addresses tough 65-nm challenges," said Brani Buric, vice president of product marketing and strategic foundry relationships at Virage Logic.

Said Rich Wawrzyniak, senior analyst at Semico Research Corp: "I am impressed with the breadth of Virage Logic's new 65-nm SiWare Memory and SiWare Logic offering and the attention to detail, in terms of providing a complete capability set."

[Virage Logic](#) is also releasing enhancements to its Self-Test and Repair (Star) memory system to address the challenges of advanced design and process technologies. Here, as well, a dashboard of user-selectable options enables tradeoffs between test time, area, and state-of-the-art diagnostics for optimal design-complexity management.

Star Yield Accelerator, another product option, expands Star's capabilities and bridges the design and manufacturing disciplines to enable automated test-vector generation, silicon analysis, fault isolation and classification to be used at the critical semiconductor tape-out, bring-up and volume manufacturing stages.

The Star Memory System will be open to enable licensees to use the system's capabilities with other commercially available and internally developed embedded memories.

"As process nodes advance, the risk and the costs of lost yield increases exponentially," noted Zorian. "With our latest release of the Star Memory System, licensees are well equipped to proceed with speed and confidence through the critical design and manufacturing stages, while optimizing the profit opportunities their products represent."

"Licensees will be offered the flexibility mixing memories from various sources and still be able to reap the benefits of the Star Memory System's capabilities," said Buric.

The Star Memory System is available at project-based pricing starting at \$25,000. Star Yield Accelerator pricing includes software and services for \$50,000.

Meanwhile SiWare IP supports major IC-design tool flows by Cadence, Magma and Synopsys, and its project pricing starts at \$70,000.

"The new developments are all based on practical data we have accumulated from real designs in the ten to 12 foundries we are working with, including TSMC and Chartered," said Zorian. "Some 75 percent of an SoC is made up of memory, so providing the capability of identifying, characterizing and classifying types of faults at the challenging 65-nm node and below can greatly affect the overall [chip](#) yield."

Virage Logic is placing its bets on continuing to serve leading-edge designs in today's tough economic waters. During the last quarter, Virage Logic consolidated some of its operations, including the closing of a Seattle R&D site.

"While we were able to grow revenue 7 percent sequentially, to \$11.3 million, we did not meet our minimum revenue guidance of \$11.5 million," said Dan McCranie, president and chief executive officer of Virage Logic, in the company's quarterly review. "Our opportunity pipeline is larger and increasing. We believe that these opportunities are a direct result of our focus, over the past six months, to develop new memory compilers and logic libraries at the most advanced process nodes, and our continuous improvement in product quality and delivery against agreed upon schedules."

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The advertisement features a blue background with a white wave graphic. On the left, there is a small image of an IGLOO FPGA chip with the text "IGLOO With Flash-Free". In the center, four surfers are riding waves. To the right, a hand holds a mobile phone displaying a surfer on its screen. The text "ARM-enabled M1 IGLOO™ FPGAs" is prominently displayed in white, followed by "Portables everywhere just got a lot cooler." in yellow. The Actel logo with the tagline "POWER MATTERS" is in the top right corner, and a yellow "» Learn More" button is at the bottom right.