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Startup spins novel core strategy

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Startup 3Plus1 Technology Inc. will emerge from stealth [mode](#) Monday (Oct. 15) with plans for silicon cores that take a "ground up" approach to accelerating media and wireless tasks. One of the company's blocks has been designed into a cell phone [chip](#) in the works at an unnamed customer who is also an investor.

The startup aims to compete with companies such as ARC and Tensilica by providing blocks that require up to 40 percent less silicon area and thus less power for specific tasks such as H.264 video [encode](#) and decode. Unlike rival cores, the 3Plus1 blocks do not include support for interrupts or other general-purpose structures and so are meant to be adjuncts to a host [processing](#) core.

3Plus1 defined 14 low-level hardware units based on a fresh analysis of the underlying processing jobs required to run today's high-growth wireless and media applications. The startup grouped those units into three functional blocks that it plans to mix and match in a set of synthesizable soft cores for licensing to makers of ASICs and standard chips.

"We are engaged with a first customer in the handset market who is taping out its first chips at the end of the quarter," said Allan Cox, chief executive of 3Plus1.

Besides video and image processing, the company claims its cores are well suited to handling [communications](#) traffic for Bluetooth, [GPS](#) or second-generation cellular networks. A block in the works for late next year is tailored for orthogonal frequency-division [multiplexing](#) to speed processing for 802.11n, Digital Video Broadcast and WiMax traffic.

"They seem to have identified some areas that are gotchas," said Richard Wawrzyniak, senior market analyst for ASICs at Semico Research (Phoenix). The analyst, who worked under Cox at Toshiba for several years, said Cox "pays a lot of attention to detail but doesn't lose sight of the big picture."

Wawrzyniak said he doesn't see 3Plus1 as a head-on competitor to ARC or Tensilica. Rather, it offers system-on-chip developers yet another option, he said. 3Plus1's "cores are not exactly CPUs, DSPs or system logic," he said, "but something with elements of all of them."

"Most competitors have a homogenous [architecture](#) with a single set of general-purpose data registers," said Kenton Williston, editor of DSP DesignLine, an affiliate of EE Times. "3Plus1 built a heterogeneous structure with different data registers for different purposes."

The architecture's data-flow-driven design "makes it easier to build multicore software because you don't have to build any supervisory code to keep everything synchronized," Williston added.

Indeed, 3Plus1 has tried to make the software shift easy for chip makers using DSP cores. General [C](#) code for DSPs can usually be ported by recompiling it on the startup's compiler. 3Plus1 offers its own software tools to enable ports to its core of the assembly language routines used for high-performance hot spots. The company claims the assembly language tools use load/store techniques similar to those found in tools provided by Texas Instruments.

The cores themselves [link](#) to the rest of a chip by either an ARM AXI or Sonics on-chip interconnect. The cores are available on standard licensing terms that include up-front fees and royalties based on volume.

Interestingly, the technical and financial strategy of the company is almost the opposite of the one pursued by failed startup QuickSilver Technology Inc., where Cox and at least one other 3Plus1 founder had been senior executives.

QuickSilver had touted a reconfigurable architecture that required users to adopt a new programming language. The company raised \$84 million before closing its doors and selling off its intellectual property.

By contrast, 3Plus1 has been funded by its founders and its initial customer, and the company has sought to minimize the changes needed in applications code.

The first two CoolEngine products from 3Plus1 use one and two instances of its CoolW core, a 128-bit-wide single-instruction, multiple-data machine aimed primarily at media applications.

The company's road map includes more cores, such as CoolIN, due late next year for OFDM processing.

It also plans to update its underlying functional units.



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