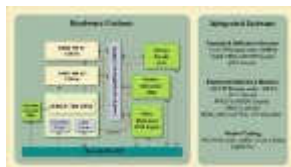


**Smart Multimedia Gallery**



 **Graphic**

The ARC Video 417V achieves high quality video encode at low power from a design comprising an ARC 700 family processor, two single instruction multiple data (SIMD) media processors and hardware accelerators for key portions of the video processing function: entropy encode (EE), entropy decode (ED), motion estimation (ME) as well as a dual-channel media-optimized direct memory access (DMA) engine. (Graphic: Business Wire)



 **Photo**

Gagan Gupta is Senior Director of Product Marketing at ARC International. Gagan is responsible for product planning and definition of ARC's multimedia subsystems and configurable processors. (Photo: Business Wire)

August 13, 2007 02:45 AM Eastern Daylight Time 

## New VRaptor™-Based ARC® Video Subsystems Set the Standard for High Quality Video Encode in Consumer Devices

*Patent Pending "Dynamic Adaptive Encoding" Technology Enables Ultra Low Power Operation to Meet Wide Ranging System Constraints*

ST. ALBANS, England--(BUSINESS WIRE)--ARC International (LSE:ARK) today set a new standard for high-quality video encoding with the introduction of five new members of the ARC® Video Subsystem family: AV 417V, AV 407V, AV406V, AV 404V, and AV 402V. All include ARC's new patent-pending technology "dynamic adaptive encoding" that enables encoding of video streams at the lowest power. The products are capable of encoding and decoding up to Standard Definition resolution video using advanced video coding standards such as H.264. The AV 417V is already shipping to customers; all are now available for licensing by companies worldwide.

ARC Video Subsystem family members enable SoC designers to quickly create unique products for a range of portable media players and tethered consumer multimedia appliances. Based on the recently introduced VRaptor™ Multicore Architecture, each is programmable, encodes and decodes a wide range of popular video standards, and comes with optimized media processing elements including:

- A member of the configurable ARC 700 core family
- Up to two 128-bit SIMD Media Processors
- A dual-channel media-optimized DMA engine
- Separate multi-standard encoding and decoding accelerators
- Programmable motion estimation accelerator
- SoC development tools
- Optimized video codecs:
  - (encoders) H.264 BP, MPEG-4 SP/ASP, H.263 profile 0, and JPEG
  - (decoders) H.264 BP, MPEG-4 SP/ASP, H.263 profile 0, VC-1 SP, MPEG-2 MP, MJPEG, JPEG, GIF, TIFF, and PNG

### The ARC® Video Subsystem Family

The new family comprises five new subsystems that are based upon the VRaptor Multicore Architecture. Features and configuration for all five are shown in the table below:

Product Feature	Configuration	Decode	Encode
AV 417V High Quality Encode/Decode	ARC 700 + 2x SIMD MP + EE + ED + ME	Up to D1	Up to D1
AV 407V Reduced Die Size Encode/Decode	ARC 700 + 1x SIMD MP + EE + ED + ME	Up to D1	Up to D1
AV 406V Low Power Encode	ARC 700 +	Up to CIF	Up to D1

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	<b>with Decode</b>	<b>1x SIMD MP + EE + ME</b>		
<b>AV 404V Low Power Decode with Encode</b>	<b>ARC 700 + 1x SIMD MP + ED +EE</b>		<b>Up to D1</b>	<b>Up to CIF</b>
<b>AV 402V Smallest Die Size Encode/Decode</b>	<b>ARC 700 + 1x SIMD MP + EE</b>		<b>Up to CIF</b>	<b>Up to CIF</b>

Legend:

SIMD MP: Single Instruction, Multiple Data Media Processor  
CIF: Common Intermediate Format, 384x288 at 30FPS  
D1 Resolution: 720x576 (TV PAL) or 720x480 (TV NTSC)  
EE: entropy encoder; ED: entropy decoder; ME: motion estimator

“ARC’s new family of VRaptor-based video subsystems represent several steps forward for designers looking to use third Party IP to craft their next silicon solution,” said Richard Wawrzyniak, senior market analyst for ASIC and SoC, at Semico Research Corp. “The subsystems’ very low power consumption coupled with high performance and very small die size make them ideal to incorporate into next generation SoCs that are trying to hit low price points. In addition, the RISC processor in these heterogeneous, multicore subsystems can function as the processing element in many applications without needing to interface to a host processor making them even more attractive. They can double as processors themselves performing computing functions other than just those specific to the target feature set.”

### High Quality Video Encode – the New Frontier in Multimedia Processing

Websites such as YouTube that enable individuals to post personally crafted video vignettes are a social phenomenon rapidly spreading around the globe. However, video quality of this content suffers from being captured by low-quality encoders that are typical in today’s camera phones and digital cameras.

With the high quality encode capability in the new ARC Video Subsystems, SoC developers can design chips that are differentiated and solve the disparate challenge of providing superior resolution encoding while consuming little power. Market opportunities for such products are booming. Research firms project the worldwide installed base of just camera phones will top 1.5 billion units by 2010, becoming the most prevalent image capture devices in the world.

### ARC – Setting the Standard in Video Quality

The top of the new line of ARC Video Subsystems is the AV 417V. Using the City video benchmark (a 30-second video clip of the Manhattan skyline) it achieves approximately a 300 percent improvement in quality compared to quality from the encoders typically found in today’s portable devices.

The ARC Video Subsystems achieve high quality video encode by employing algorithms (“tools”) specified from standards bodies for video codecs such as H.264, which is up to five times more complex than other coding standards. Their high performance architecture (based on VRaptor) allows usage of the demanding encoding algorithms at reasonable clocking frequency resulting in a power-efficient solution.

The AV 417V Subsystem occupies just 4.95 mm<sup>2</sup> in a 90nm process technology and achieves the following encode and decode performances:

- H.264 BP encode of D1, 30 fps video stream of up to 10 Mbps bit rate, operating under 200 MHz
- H.264 decode of D1, 30 fps video stream of 1.5Mbps bit rate, operating at 160 MHz

### Low Power Via ARC’s New “Dynamic Adaptive Encoding” Technology

A major innovation embodied in the new members of ARC's Video Subsystem Family is the patent pending technology called Dynamic Adaptive Encoding. The technology encodes video optimally under any system condition. Video encoding is a repetitive task that executes a set of algorithms to encode a digitized video stream or a set of digitized still images into such standards as H.264 BP, MPEG-4 SP/ASP, H.263 profile 0, and JPEG. Dynamic Adaptive Encoding continuously evaluates system resources and adaptively applies different processing resources to achieve the optimum result. For example, dynamic adaptive encoding allows the designer to adjust the encoding process in a phone with a fully charged battery versus one running close to empty.

### **ARC Video Subsystems – A New Way to Differentiate SoCs**

Un-optimized, general purpose CPUs and DSPs cannot efficiently process complicated multimedia algorithms. Therefore, SoC designers typically have to implement numerous general purpose cores on a chip resulting in exploding silicon footprints and high power consumption. This approach is less than ideal for portable applications.

Alternatively, dedicated fixed-function hardware blocks are used to process specific media algorithms. However, this approach offers no programmability to adapt to evolving codec standards thereby limiting the product's life span. ARC's Video Subsystems are uniquely optimized to the special processing needs of video and audio applications. They are as follows:

- Programmable to handle multi-format codecs and additional user-specific applications
- Configurable to enable maximum product differentiation
- Pre-integrated and pre-verified to eliminate much of the software and hardware design effort
- Efficient video encode using very low power and little silicon real estate

### **ARC VRaptor™ Multicore Architecture**

The new members of the ARC Video Subsystem family are based upon the recently introduced VRaptor Multicore Architecture. It is a scalable heterogeneous processor architecture that overcomes the performance challenge of low power multimedia processing. VRaptor provides three distinct classes of ARC core modules. The first class includes a configurable 700 family core, and a range of specialized SIMD multimedia processors optimized for functions such as low-pass deblocking filters and pixel transforms. The second class includes accelerators, such as entropy encoders and decoders and motion estimators. These perform multimedia processing tasks more efficiently than general-purpose, programmable cores. And the third class includes high speed DMA controllers to relieve the CPU from complex data movement often found in multimedia codecs.

Connecting VRaptor's heterogeneous multicore resources together is its unique remote procedure invocation over communication channels capability. The 700 processor core, SIMD accelerators, DMA engine, entropy encoders and decoders, and motion estimation accelerators are all loosely coupled and operate independently of one another. The 700 processor core apportions work to each of the accelerators using a simple fire-and-forget message. The message in main memory enables a zero overhead context switch that directs the accelerator to perform a task and inform the 700 processor when complete, at which time the 700 processor immediately issues the accelerator another context switch that initiates another task. In this manner all the accelerators are kept running independently at full speed without having to await the result of any other processing resource in the system.

### **Availability**

The ARC Video Subsystem family is now available for licensing by companies worldwide. For more information contact ARC International at [info@arc.com](mailto:info@arc.com) or visit [www.arc.com](http://www.arc.com).

### **About ARC International plc**

ARC International is the world leader in configurable media subsystems and CPU/DSP processors. Used by over 140 companies worldwide, ARC's configurable solutions enable the creation of highly differentiated system-on-chips (SoCs) that ship in hundreds of millions of devices annually. ARC's patented subsystems and cores are smaller, consume less power, and

are less expensive to manufacture than competing products.

ARC International maintains a worldwide presence with corporate and research and development offices in Silicon Valley and St. Albans, UK. For more information visit [www.ARC.com](http://www.ARC.com). ARC International is listed on the London Stock Exchange as ARC International plc (LSE:ARK).

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### At A Glance

#### ARC International

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Employees:	130
Ticker:	ARK (LSE)
Revenues:	N/A (2004)
Net Income:	N/A (2004)

*Source: via Business Wire  
Updated 11/23/2004 by company*

