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TSMC lifts lid on 45-nm design methodology

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Seeking to make a big splash at the Design Automation Conference in [San](#) Diego this week, Taiwan Semiconductor Manufacturing Co. Ltd. today will unveil its latest and most ambitious design methodology for IC production at the challenging 45-nanometer node.

Reference Flow 8.0, a collection of design tools and technologies optimized for TSMC's new 45-nm foundry process, represents a mammoth

collaboration between the foundry giant and a slew of EDA vendors that addresses a potentially worrisome issue: how to move expensive 45-nm designs into production without [circuit](#) failures, mask respins or other costly problems. Other leading-edge foundries are working on similar flows.

At 45 nm, IC design costs are expected to reach \$30 million or more. Photomask costs are also soaring out of control. With those and other costs in mind, there is little room for error in IC design and production, commented Rich Wawrzyniak, an analyst for Semico Research Corp. For startups, he said, "it's almost getting to the point that if a product fails, the company could also fail." And for larger companies, the temptation is to play it safe by taking fewer design risks.

To combat those trends, leading-edge foundries must ensure that their respective 45-nm processes are production-worthy. In fact, foundries are under increasing pressure not only to develop the costly process technologies, but also to provide more of the pieces of the IC design puzzle. Those include a wider range of third-party EDA tools, intellectual-property (IP) blocks, libraries and, of course, design flows. In other words, the foundries are expected to put more resources into bridging the gap between design and manufacturing.

"Each time you go down a process node, there are more issues involved," said Tom Quan, deputy director of design services at TSMC's U.S. unit, TSMC North America. That, in turn, requires more "collaboration in the design ecosystem."

Go with the flow

That is what TSMC did in creating the 8.0 flow. In a departure from its previous offerings, the flow calls for TSMC to share and license select proprietary production data--its "secret sauce"--with customers in an effort to span the breach between design and manufacture.

The suite also gives a ringing endorsement to Cadence Design Systems Inc.'s low-power EDA standard, dubbed the Common Power [Format](#) (CPF). And compared with TSMC's Reference Flow 7.0, the 8.0 version supports more advanced techniques, including statistical timing analysis for intradie variation, automated design-for-manufacturing (DFM) hot-spot fixing and dynamic low-power design. It also adds support for the company's [IP](#) program.

The result is a "seamless [link](#) between designers and advanced process technologies" at 45 nm, said Kuo Wu, deputy director of design service marketing at TSMC.

The flow also accelerates time-to-market for the new 45-nm process, Wu said. TSMC officially rolled out its 45-nm process technology for foundry customers in April, with plans to enter production as early as September. Rival foundry vendors--Chartered, IBM, Samsung and UMC--are separately expected to move into 45-nm production around the end of the year.

The question is whether the leading-edge foundries can deliver 45-nm processes without hiccups. The 45-nm node represents the first time they will use 193-nm immersion lithography and ultralow-k dielectrics.

One enabler for foundry customers is the advent of design guidelines or standard reference flows, which consist of a complex array

of internal and third-party EDA tools. As the industry has moved to finer [chip](#) geometries, design flows have become more sophisticated and more crucial for foundry customers.

"What's surprising about this announcement is that TSMC has updated its reference flow so fast," said Gary Smith, chief analyst at Gary Smith EDA.

The effort comes out of TSMC's critical but overlooked design services group. Over the past five years, TSMC has spent \$100 million on R&D in that group alone.

Up until the 130-nm node, TSMC provided customers with full-chip layout and other services. But because of the low margins, the foundry giant has "handed off that work to the fabless companies," Smith said.

Instead, TSMC is paying more attention to the development of reference flows, design blocks and IP. Indeed, one of the company's more controversial efforts is in the IP arena, where TSMC's internal IP appears to compete against that of third-party IP vendors. TSMC insists its IP efforts are complementary, not competitive, with the work of its IP partners (see April 23, page 1).

This week, the foundry provider will formally announce a new part of its IP program, the Active Accuracy Assurance initiative. AAA provides "standards of accuracy" and stringent guidelines for all TSMC partners, including EDA vendors, IP providers and [library](#) developers.

TSMC applies those same standards to its reference flows, tools and process design kits.

Perhaps the bigger announcement involves the contents of TSMC's Reference Flow 8.0. The design methodology consists of many of the same elements as the previous, 7.0 version: timing closure, hierarchical flow, silicon flow, power closure flow, enhanced power management, enhanced DFM and statistical timing. But 8.0 expands the foundry's efforts in DFM, power management and statistical timing analysis.

TSMC's design methodology is a guideline that involves various collaborations with EDA, DFM and IP houses. The foundry has qualified dozens of IP houses within its AAA program, and its DFM [Compliance](#) Initiative--which focuses on the design-for-manufacturability portion of the design ecosystem--has grown from 15 to 20 tool vendors. The world's largest foundry has alliances with Alchip, [Analog](#) Bits, Anchor, Aprio, ARM, Blaze, Cadence, Clear Shape, Dolphin, eSilicon, Fasttrack, Global Unichip, Magma, Mentor, Open-Silicon, Ponte, Predictions, Think, Silicon Canvas, Synopsys and Virage.

Cadence, Mentor and Synopsys are providing the DFM utilities at 45 nm. TSMC has also qualified other EDA vendors--Clear Shape, Magma, Ponte and Predictions Software--at the 45-nm node for DFM. For statistical timing analysis, TSMC is working with Cadence, Magma and Synopsys, each of which is providing a suite of tools.

The 7.0 reference flow incorporated a DFM unified format as the foundation for TSMC's tool compliance program. As part of the 8.0 flow, TSMC plans to license its proprietary DFM unified format technology to the outside industry. In addition, the foundry will provide select proprietary manufacturing data via encrypted DFM data kits.

New to TSMC's DFM methodology are automated DFM [hotspot](#) fixing, to eliminate the need for manual correction, and DFM electrical-variability consideration, which will [monitor](#) parametric performance shifts caused by DFM effects.

Power management is another hot topic. In the 45-nm flow, TSMC will implement Cadence's CPF technology to automate the low-power design methodology. But at some point, it is also expected to endorse a rival low-power technology, Accellera's Unified Power Format, said Smith of Gary Smith EDA.

TSMC provides three low-power management technologies within the flow: dynamic power, active leakage and standby leakage. One new technique in the dynamic-power category is adaptive voltage scaling. Offered in the form of process-monitoring blocks, the technology reduces [voltage](#) within the IP by 10 to 15 percent, TSMC's Quan said.

For active leakage, TSMC provides a new long-channel device technique. It has also added coarse-grained power gating in its standard cells in a bid to reduce overall standby leakage.



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