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## Seminars explain SoC memory designs

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**Technical seminars address techniques for designing today's DDR2 SDRAMs into SoC applications, and the future for DDR3 memories**

Semico Research, Fidus Systems and Mosaid Technologies are hosting technical seminars on designing today's **DDR2 SDRAMs into SoC applications, and the future for DDR3 memories**. Titled 'SoC forum - designing for DDR SDRAMs and the outlook for DDR3', the free half-day seminars will be held worldwide in February and March 2007.

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SoC designs increasingly rely on DDR as an interface to an external memory.

Although DDR2 SDRAM offers security of supply, high storage capacity, low cost and ample channel bandwidth, it is an awkward interface at both the logical and physical levels and faces complicated controller issues.

Designers will learn about effectively interfacing SoC designs to off-chip DDR SDRAMs.

'SoC designers often face a daunting task when incorporating a modern DRAM interface into their design', said Michael Kaskowitz, Senior Vice President, Semiconductor IP, Mosaid.

'Our technical seminar addresses this by examining the entire process of designing SoCs with DRAM interfaces, from inception through completed PCB and beyond'.

Presenting will be: Mike Wakim, President and CEO, Fidus; Bob Merritt, Vice President, DRAM, Semico; Peter Gillingham, Vice President and CTO, Mosaid; and Graham Allan, Director of Marketing, Semiconductor IP, Mosaid.

Topics include: **DDR memory** as a key enabler for next-generation consumer electronics ICs; high-performance **DDR memory controller** issues; integrating DDR SDRAMs for PCB success; and an overview of the **DDR SDRAM** roadmap, looking to DDR3.

The seminar series begins on 21st February 2007 in Herzliya, Israel, and continues via the USA, Taiwan and China to conclude in Tokyo, Japan on 23rd March 2007.

Full details of venues and registration information can be found on the Mosaid website.

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