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Last semi roadblock cleared?

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PORTLAND, Ore. — Startup Mears Technologies claims to have cleared one of the last remaining roadblocks in a chip industry roadmap for extending Moore's Law down to the 22-nanometer node: gate leakage.

By modifying the transistor channel, Mears claims its technique enables Moore's Law to continue unabated to the 22-nm node. The technique works by blocking gate leakage with a silicon superlattice called silicon-on-silicon.

The shift is one of the key roadblocks to achieving the goals of the International Technlogy Roadmap for Semiconductors.

"The biggest problem with going below 65 nanometers is gate leakage, and Mears appears to have a solution to it," said Morry Marshall, vice president of stategic technology at Semico Research Corp. (Phoenix). "If it works like Mears claims, then there should be instant adoption by the industry. The only thing that could prevent its adoption is conservatism, skepticism and [the] not-invented-here syndrome."

Mears Technologies (Waltham, Mass.) claims its superlattice enhances carrier mobility in the channel plane while simultaneously blocking gate leakage, which is vertical to a chip's plane.

"They are putting down monolayers, some of which are highly conductive, but they alternate with layers that block currrent flow in the vertical direction, thereby mitigating gate leakage," said Trevor Yancey, vice president of technology, IC Insights Inc. (Scottsdale, Ariz.).

Mears claims its superlattice can be added to existing CMOS processes in a few extra steps during transistor channel growth.

The semiconductor roadmap seeks to pool chip-making resources to solve problems thwarting the advance of Moore's Law. At lower nodes, obstacles are growing, prompting many analysts to predict a slowing of Moore's Law beyond 130 nm.

"Prior to strained silicon, the outlook was pretty bleak—no one could see how to keep improving performance while simultaneously cutting power consumption," said Semico's Marshall.

Strained silicon reduces the effective mass of electrons, thereby increasing mobility and enabling the transition to 65 nm. Silicon-on-insulator also enhances CMOS circuitry performance at the 65-nm node by electrically isolating adjacent devices and allowing for innovative device layouts.

But neither technique addresses gate leakages, which could potentially be mitigated using high-K dielectrics or even metal gates. Mears focused instead on superlattices.

"We instead can improve the baseline on [high-K dielectrics and SOI] by pushing the power and performance equation," said Mears' CEO-designate Neil Vasant. "Our technology can be added to strained silicon, SOI or even bulk CMOS, and the other technologies can fit right alongside ours over the next five or ten years as they become ready for production."

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