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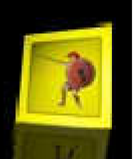

Embedded superlattice slashes gate leakage

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PORTLAND, Ore. — CMOS devices isolate transistor gates from their channels with supposedly impenetrable oxides. But as chips scale below the 65-nanometer node, those oxides become so thin that applying enough voltage to turn on a transistor also enables a percentage of the electrons charging the gate to tunnel through the oxide into the channel.

"CMOS was originally adopted because it was considered to be a zero-leakage technology," said Robert Mears, founder, president and chief technology officer of Mears Technologies (Waltham, Mass.). "But gate leakage now dominates power consumption below 65 nanometers," where it can account for 70 percent of power consumed. "And as you go down the nodes, the problem only gets worse."

Mears Technologies addresses the leakage problem by adding an embedded superlattice during the construction of a transistor's channel to enhance current flow in the plane of the channel, while simultaneously blocking current flow perpendicular to the channel, thereby mitigating gate leakage. It claims its sili- con-on-silicon superlattice can reduce gate leakage by 70 to 90 percent, while increasing current drive in the channel. Founded in 1999, the company has filed 150 patents for technologies related to eliminating gate leakage.

"Gate leakage is absolutely the major problem in going to the lower nodes, and Mears appears to have an elegant solution," said Trevor Yancey, vice president of technology at IC Insights Inc. (Scottsdale, Ariz.).

Semiconductor makers have turned to new materials and exotic processing step to quell gate leakage, but Mears Technologies claims its solution is straightforward and simple.

"If Mears' technology works the way they claim it does, then it's the solution to the gate leakage problem that everyone has been looking for," said Morry Marshall, vice president of strategic technology at Semico Research Corp. (Phoenix, Ariz.). "The alternatives to Mears' technology are uncertain, expensive or outright dicey."

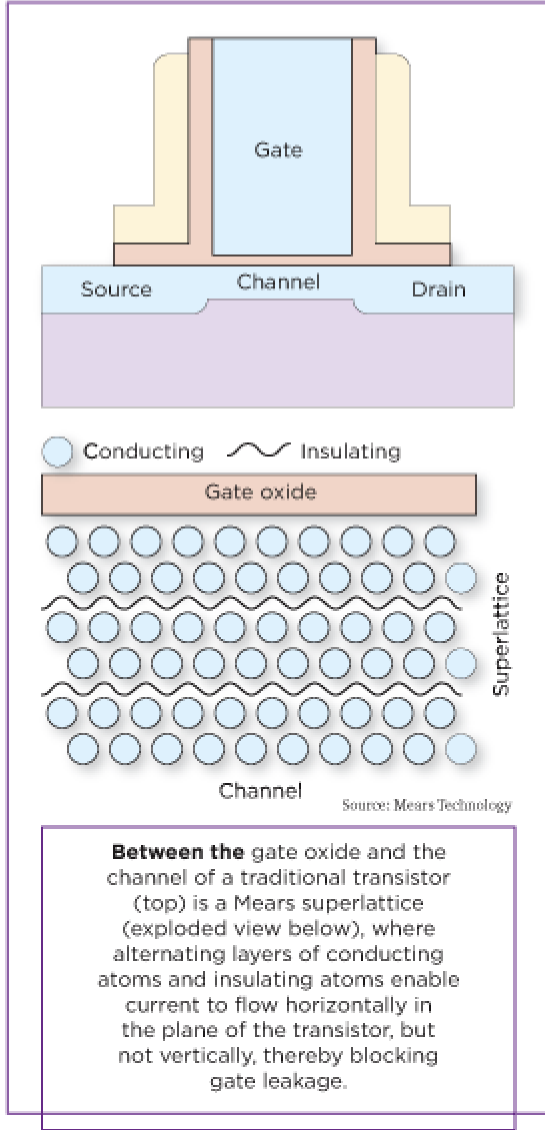
Those other alternatives, as proposed by the International Technology Roadmap for Semiconductors, address gate leakage with high-k dielectric oxides that insulate better, or with gates made from highly conductive metals. But transitioning to the new materials is so risky that mainstream semiconductor makers have delayed their introduction, which had been slated for 65 nm.

Mears' approach, which tweaks the existing construction methodology for the transistor channel, does not require new materials and can be added without increasing the cost of the chips, the company claims. Mears says use of its solution could extend Moore's Law at least to 22 nanometers and potentially all the way to the atomic scale.

Add it on

Mears Technologies claims its technique can be added to existing processes, including ones that have already adopted other measures to achieve performance goals at 65 nm.

Those alternatives include strained silicon, which enhances electron mobility in the transistor channel. "Strained silicon [splits] the degeneracy between light and heavy holes, or the equivalent in the conduction band, and thereby gives you a lower effective mass and higher mobility in the plane of the device," said Mears. "At 90 nm, strained silicon was successfully introduced to meet performance requirements, but as you scale down, it becomes increasingly difficult to get the same sort of performance enhancements from stained silicon."



Between the gate oxide and the channel of a traditional transistor (top) is a Mears superlattice (exploded view below), where alternating layers of conducting atoms and insulating atoms enable current to flow horizontally in the plane of the transistor, but not vertically, thereby blocking gate leakage.

Others have opted to use silicon- on-insulator (SOI), which achieves lower parasitic capacitance and re- duced junction leakage by virtue of an embedded oxide layer that effectively isolates transistors from each other. But like strained silicon, SOI has limitations below 65 nm. And neither strained silicon nor SOI directly addresses the problem of gate leakage.

Mears Technologies' technique involves inserting "epitaxially grown silicon into a standard CMOS flow as a channel replacement layer. The net result of is two-dimensional, sheet-like behavior, compared with standard, 3-D epitaxial silicon," said Mears.

Called silicon-on-silicon, the structure is basically a superlattice laminate, about 100 angstroms thick, in which the silicon atoms are spaced out slightly more in the vertical direction than in the plane of the device, thereby creating channels for electrons and holes to travel parallel to the surface more easily, while blocking vertical conduction between the gate and the channel.

"In the plane of the device, the electron density is more distributed or delocalized, thereby achieving a lower effective mass or a higher mobility in that plane," Mears said. "But in the vertical direction, this material is anisotropic [using an etch rate in the direction parallel to the surface that is lower than the etch rate used in the direction perpendicular to the surface], giving it a higher effective mass and lower conductivity in the vertical direction. That gives our technology its inherent gate leakage reduction capability."

"They are putting down mono- layers, some of which are highly conductive, and they alternate with layers that act to prevent the gate leakage that occurs in the vertical direction," said IC Insights' Yancey.

The superlattice merely adds a few processing steps to the process for making normal transistor channels. Adopters thus can easily insert the extra steps without upsetting their current processes or their plans for extending those processes down to 22 nm, according to the company.

"The industry is crafting many technologies to get to 45 nanometers, and all of those can be fit to our platform," said Neil Vasant, CEO designate at Mears Technologies. "For those who already have strained silicon or SOI, our technology brings yet another layer of benefit and investment return by squeezing out yet more performance or further lowering power consumption."

Since no new materials need be introduced to use Mears Technologies' channel replacement technology, it can be added to fabrication facilities with a minimum of fuss. For its tests, Mears Technologies used standard development and production tooling on an ASM Epsilon 2000. That single-wafer epitaxial reactor series is readily available, with more than 500 units said to be operating in the field.

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